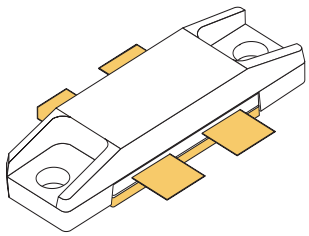
STAC9200

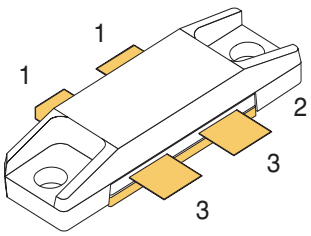
200 W, 32 V HF to 1.3 GHz LDMOS transistor in a STAC package

Datasheet - preliminary data



STAC244B
Air cavity

Figure 1. Pin connection



1. Drain
2. Source (bottom side)
3. Gate

Features

- Improved ruggedness: $V_{(BR)DSS}$ > 80 V
- Load mismatch 65:1 all phases @ 200 W / 32 V / 860 MHz under 1 msec - 10%
- P_{OUT} = 200 W min. (250 W typ.) with 16 dB gain @ 860 MHz
- In compliance with the 2002/95/EC European directive
- ST air-cavity STAC® packaging technology

Description

The STAC9200 is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for broadband applications in the HF to 1300 MHz frequency range. The STAC9200 benefits from the latest generation of efficient STAC® package technology.

Table 1. Device summary

Order code	Marking	Package	Packaging
STAC9200	STAC9200(1)	STAC244B	Plastic tray

1. For more details please refer to *Chapter 8: Marking, packing and shipping specifications*.

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction-case thermal resistance	0.525	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 4. Static (per side)

Symbol	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 10 mA	80			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 28 V			1	µA
I_{GSS}	V_{GS} = 15 V	V_{DS} = 0 V			1	µA
$V_{GS(Q)}$	V_{DS} = 10 V	I_D = 250 mA	2.0		4.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 3 A			0.8	V
G_{FS}	V_{DS} = 10 V	I_D = 3 A	2.5			S
C_{ISS}	V_{GS} = 32 V	f = 1 MHz		113		pF
C_{OSS}	V_{DS} = 32 V	f = 1 MHz		57		pF
C_{RS}	V_{DS} = 32 V	f = 1 MHz		1.2		pF

2.2 Dynamic

Table 5. Dynamic(1)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	P_{IN} = 5 W	200	230	-	W
h_D	P_{IN} = 5 W	60	68	-	%
Gain	P_{OUT} = 200 W		18	-	dB

1. Freq = 860 MHz / V_{DD} = 32 V / I_{DQ} = 0.1 A.

3 Impedance

Figure 2. Current conventions

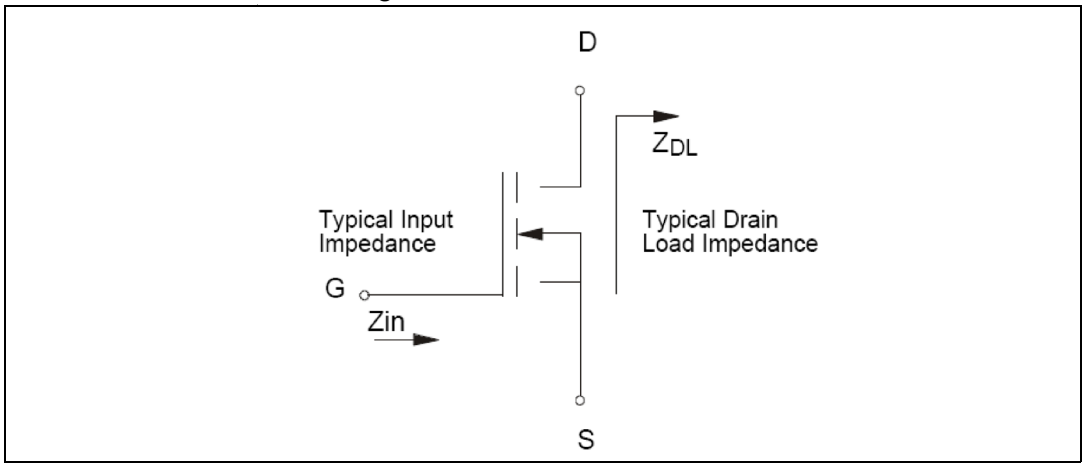


Table 6. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
200	TBD	7.63 + j 2.92
280	TBD	7.02 + j 3.82
360	TBD	6.34 + j 4.52
440	TBD	5.66 + j 5.05
520	TBD	5.01 + j 5.43
600	TBD	4.42 + j 5.70
700	TBD	TBD
800	TBD	TBD
860	2.04 + j 5.33	2.33 + j 3.02
900	TBD	TBD
1000	TBD	TBD

Note: Measured gate-to-gate and drain-to-drain, respectively.

4 Typical performance

Figure 3. Output power and efficiency versus input power

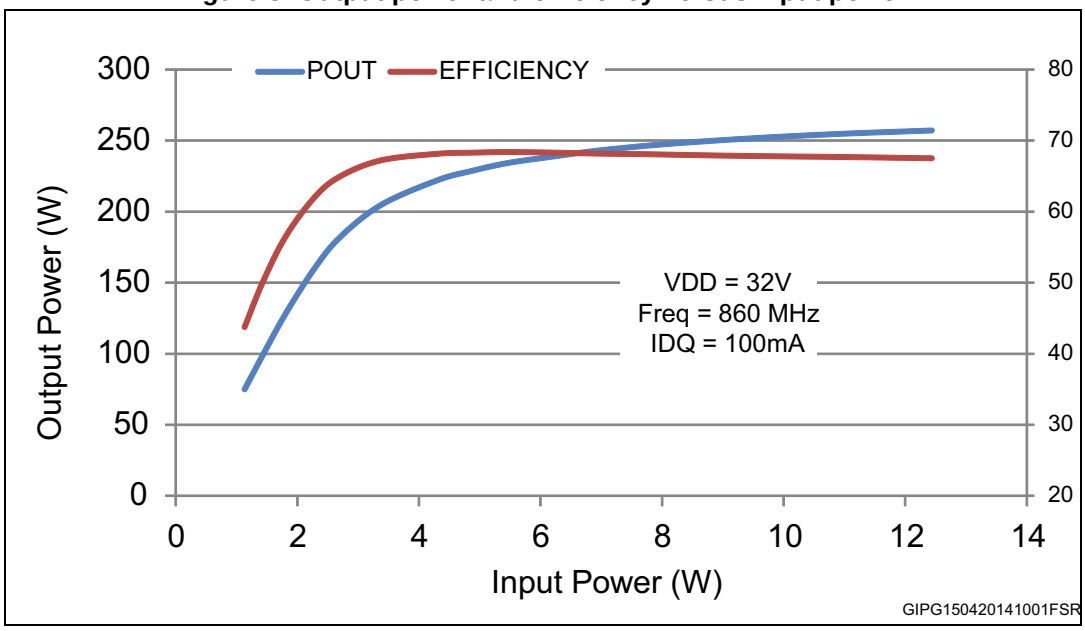
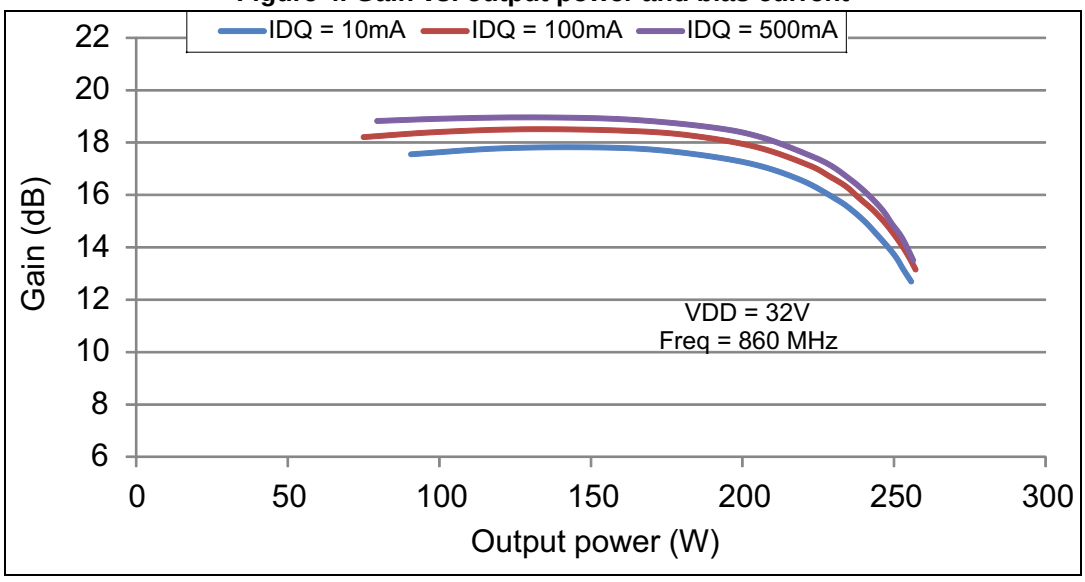


Figure 4. Gain vs. output power and bias current



5 Electrical schematic and BOM

Figure 5. Electrical schematic

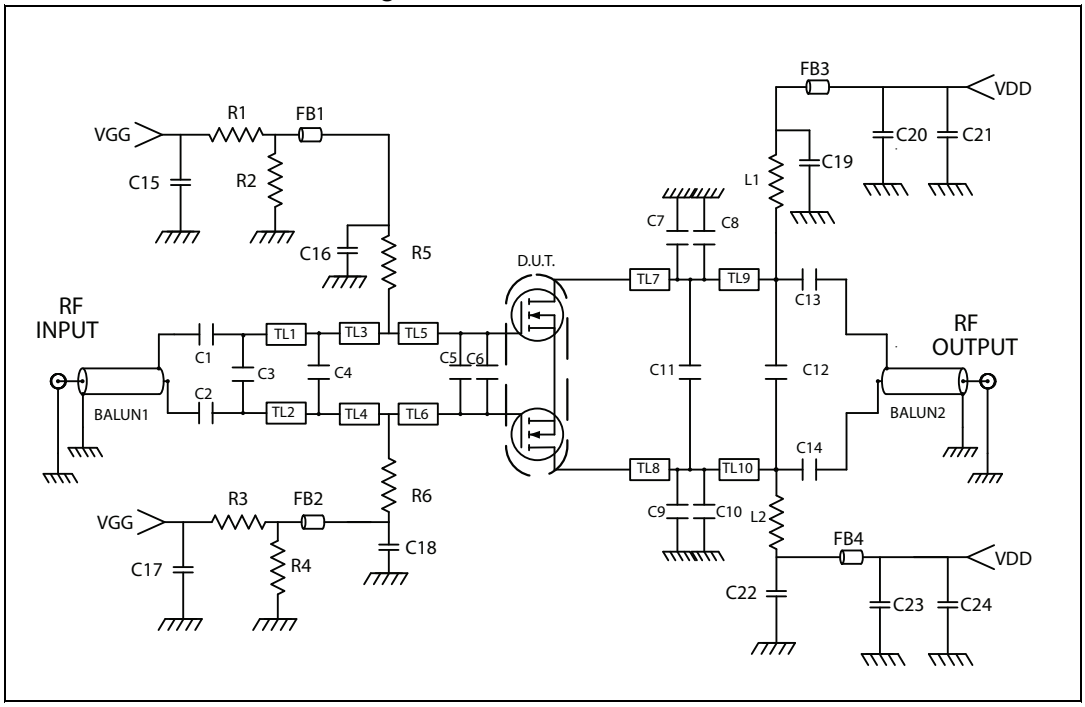


Table 7. Component list

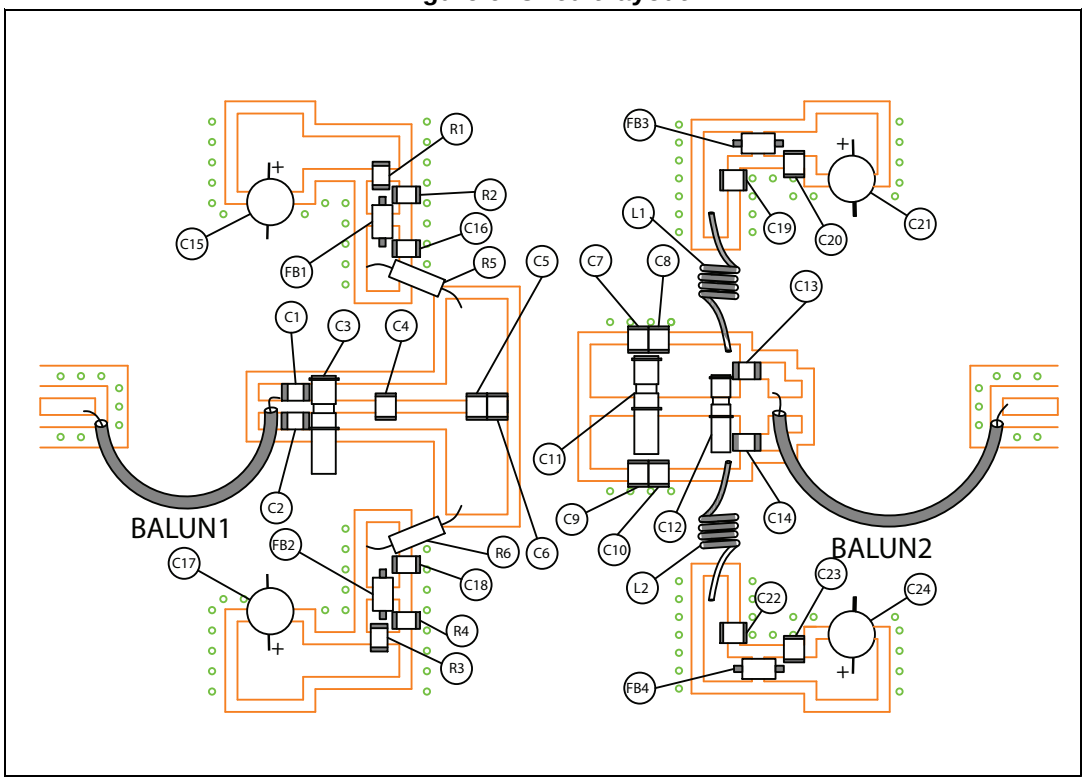
Item	Qty	Part no	Vendor	Description, dimension (x,y)
C1,C2,C13,C14, C16,C18,C19,C22	8	ATC100B510FW1500X	ATC	51 pF ATC 100B surface mount ceramic chip capacitor
C3, C11	2	27291PC	JOHANSON	0.8-8 pF Giga trim variable capacitor
C4	1	ATC100B0R6BW1500XT	ATC	0.6 pF ATC 100B surface mount ceramic chip capacitor
C5	1	ATC100B6R2BW1500XT	ATC	6.2 pF ATC 100B surface mount ceramic chip capacitor
C6	1	ATC100B150BW1500XT	ATC	15 pF ATC 100B surface mount ceramic chip capacitor
C7,C9	2	ATC100B5R1BW1500XT	ATC	5.1 pF ATC 100B surface mount ceramic chip capacitor
C8,C10	2	ATC100B4R7BW1500XT	ATC	4.7 pF ATC 100B surface mount ceramic chip capacitor
C12	1		JOHANSON	0.6-4.5pF Giga trim variable capacitor
C15,C17	2	SEK101M063ST		100 µF, 63V electrolytic capacitor
C20,C23	2	ATC200B393KW50X	ATC	39.000 pF ATC 200B surface mount ceramic chip capacitor

Table 7. Component list (continued)

Item	Qty	Part no	Vendor	Description, dimension (x,y)
C21,C24	2	UPW1H222MHD		2200 µF, 50V aluminum electrolytic capacitor
B1,B2	2	EZ141	HUBER-SUHNER	BALUN, 50 OHM SUCOFORM, OD 0.141. 2.12 LG coaxial cable or equivalent
L1, L2	2		BELDEN	INDUCTOR, 4 turns air-wound #18AWG ID=0.13in
R1,R3	2	CR1206-8W-911JB	VENKEL	0.91 K OHM surface mount chip resistor
R2,R4	2	CR1206-8W-914JB	VENKEL	910 K OHM surface mount chip resistor
R5,R6	2	RCO7GF510J	Allen Bradley	51 OHM 1/4W carbon composition resistor
FB1,FB2,FB3,FB4	4	2743021447	FAIR-RITE CORP	Surface mount emi shield bead
TL1,TL2				L= 0.414in W=0.082in
TL3,TL4				L= 0.297in W=0.082in
TL5,TL6				L= 0.302in W=0.500in
TL7,TL8				L= 0.385in W=0.260in
TL9,TL10				L= 0.350in W=0.260in
Board 3X5	1		Rogers Corp	0.030 THK , Er=2.5, 2Oz Cu both sides

6 Circuit layout

Figure 6. Circuit layout



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 7. STAC244B package outline

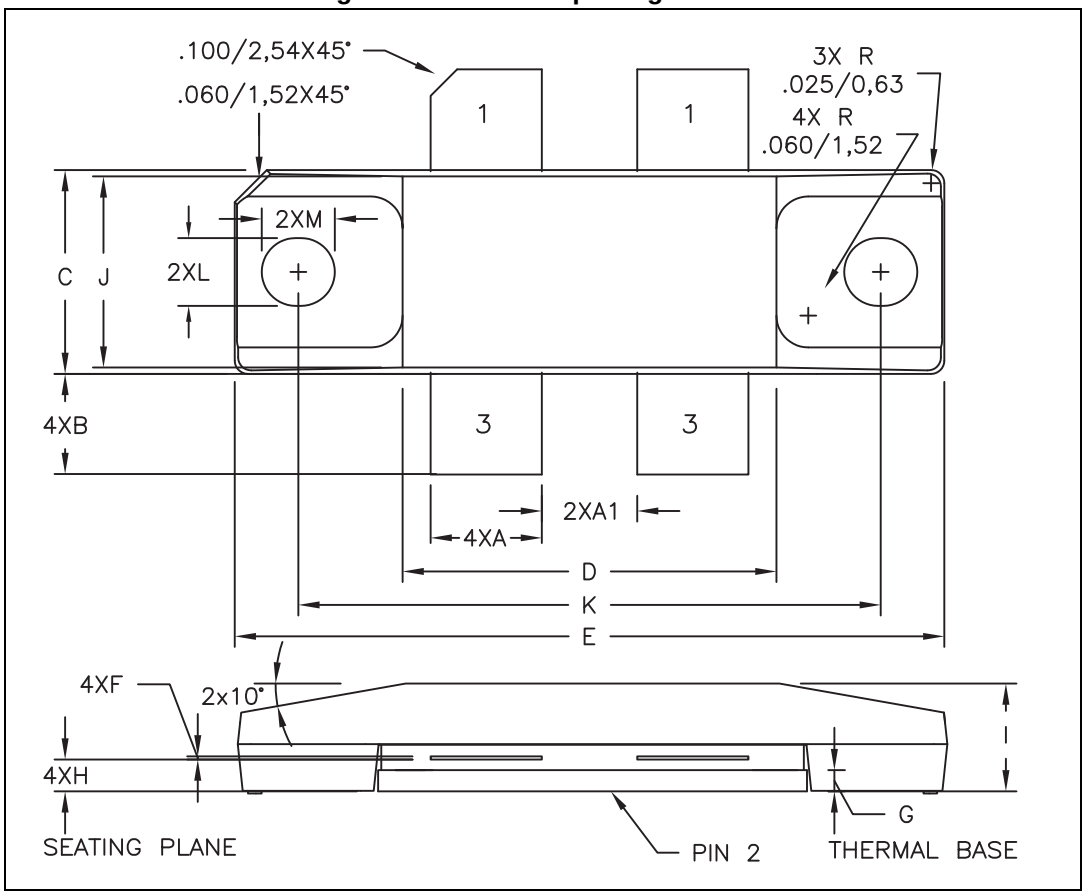


Table 8. STAC244B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.08		5.59
A1	4.32		4.83
B	4.32		5.33
C	9.65		9.91
D	17.78		18.08
E	33.88		34.19
F	0.10		0.15
G		1.02	
H	1.45		1.70
I	4.83		5.33
J	9.27		9.52
K	27.69		28.19
L	3.12	3.23	3.33
M	3.35	3.45	3.56

8 Marking, packing and shipping specifications

Table 9. Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	Lot code
STAC9200	Tray	20	< 10%	Two codes max

Figure 8. Marking layout

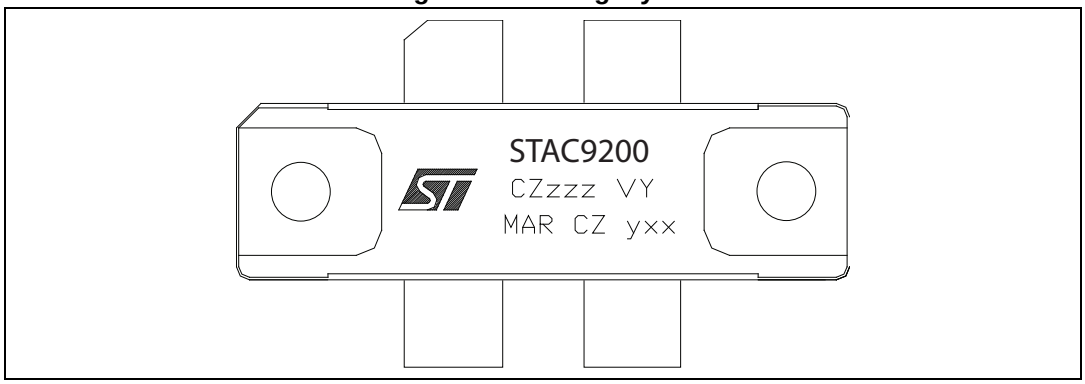


Table 10. Marking specifications

Symbol	Description
CZ	Assembly plant
zzz	Last 3 digits of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assembly year
xx	Assembly week

9 Revision history

Table 11. Document revision history

Date	Revision	Changes
21-Oct-2013	1	First release.
22-Apr-2014	2	Updated features in cover page, Table 4: Dynamic and Table 5: Impedance data. Added Section 4: Typical performance, Section 5: Electrical schematic and BOM and Section 6: Circuit layout.
10-Nov-2015	3	Added *Section 1.2: Thermal data*. Minor text changes.