QPA2626D

17 – 23 GHz Low Noise Amplifier

Product Overview

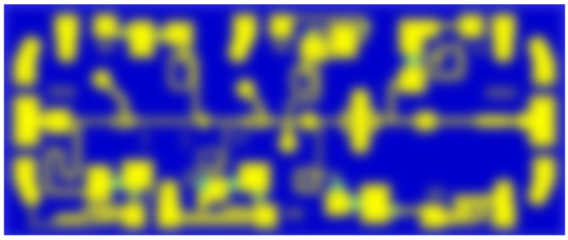
Qorvo's QPA2626D is a high-performance, low noise MMIC amplifier fabricated on Qorvo's production 90nm pHEMT process (QPHT09). Covering 17 – 23 GHz, the QPA2626D provides 25 dB small signal gain and P1dB of 20 dBm, while supporting a noise figure of 1.3 dB and IM3 levels of –55 dBc (at Pout=0 dBm/tone).

The QPA2626D is matched to 50 ohms with integrated DC blocking caps on both I/O ports for easy handling and simple system integration.

The high performance of the QPA2626D makes it ideal for satellite and point to point communication systems.

Lead-free and RoHS compliant.

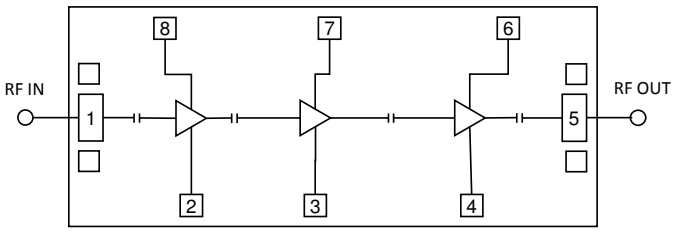
Evaluation boards are available upon request.



Key Features

- Frequency Range: 17 – 23 GHz
- Noise Figure: 1.3 dB (typical)
- Small Signal Gain: 25 dB (typical)
- P1dB: 20 dBm (typical)
- IM3: –55 dBc (typical) (Pout=0 dBm/tone)
- Bias: VD = 3.5 V, IDQ = 90 mA, VG = –0.46 V (typical)
- Die Dimensions: 2.40 x 1.00 x 0.10 mm

Functional Block Diagram



Top View

Applications

- Satellite Communications
- Point-to-Point Communications

Ordering Information

Part No.	ECCN	Description
QPA2626D	EAR99	17 – 23 GHz Low Noise Amplifier
QPA2626D_EVB	EAR99	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_D)	5.0 V
Drain Current (I_{D1}/I_{D2}/I_{D3})	45/45/160 mA
Gate Voltage Range (V_G)	–1.5 V to 0 V
Gate Current (I_{G1}/I_{G2}/I_{G3} at 125 °C)	5.0/5.0/6.6 mA
RF Input Power (50 Ω, 85 °C)	20 dBm
Channel Temperature, T_{CH}	175 °C
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	–55 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Typ	Units
Drain Voltage	3.5 V	V
Drain Current (quiescent, I_{DQ})	90 mA	mA
Drain Current (I_D, Low noise / P_{SAT})	90 / 175 mA	mA
Gate Voltage (typical)	–0.46 V	V
Operating Temperature Range	–40 to 85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

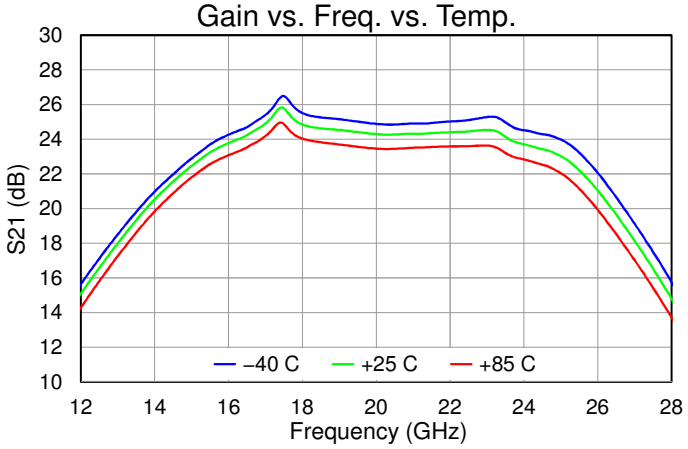
Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C. Data de-embedded to MMIC bond wires.

Parameter	Conditions [1]	Min	Typ	Max	Units
Operating Frequency		17		23	GHz
Small Signal Gain	17.0 GHz 20.0 GHz 23.0 GHz		25.0 24.5 24.5		dB
Noise Figure	17.0 GHz 20.0 GHz 23.0 GHz		1.3 1.1 1.5		dB
1-dB Compression Point	17.0 GHz 20.0 GHz 23.0 GHz		14.5 19.5 21.5		dBm
Input Return Loss	17.0 GHz 20.0 GHz 23.0 GHz		11.0 7.0 8.0		dB
Output Return Loss	17.0 GHz 20.0 GHz 23.0 GHz		6.0 11.0 13.0		dB
3RD Order Intermodulation Level (P_{OUT} = 0 dBm / Tone)	17.0 GHz (P_{OUT} = 0 dBm / Tone) 20.0 GHz (P_{OUT} = 0 dBm / Tone) 23.0 GHz (P_{OUT} = 0 dBm / Tone)		–42.0 –54.0 –60.0		dBc
Output TOI	17.0 GHz 20.0 GHz 23.0 GHz		21.0 26.5 30.0		dBm
Gain (S21) Temperature Coefficient			–0.008		dB/°C

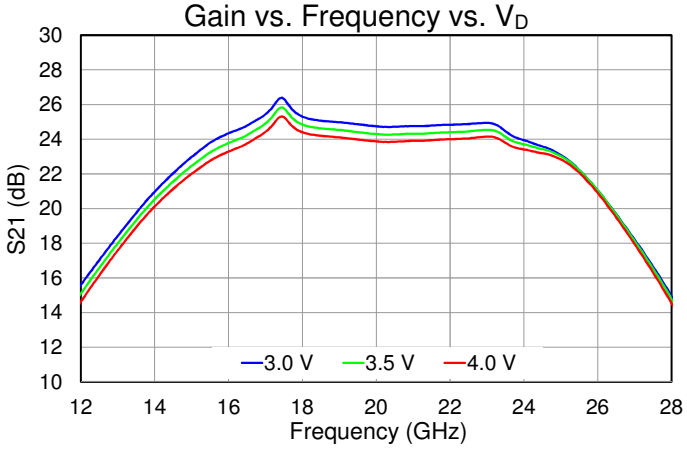
Performance Plots – Small Signal

Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C. Data de-embedded to MMIC bond wires.

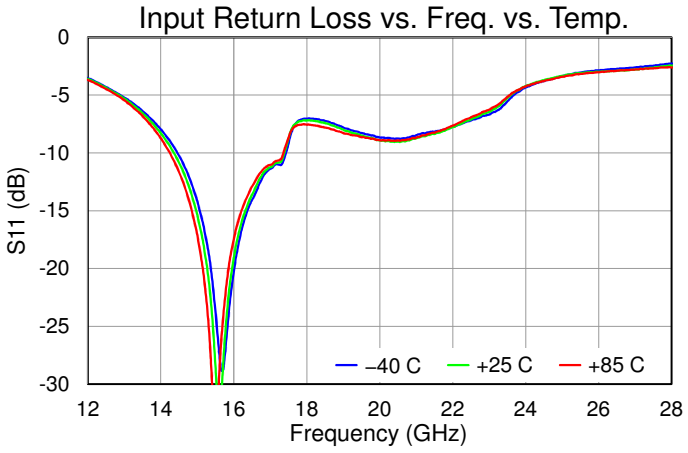
Gain vs. Freq. vs. Temp.



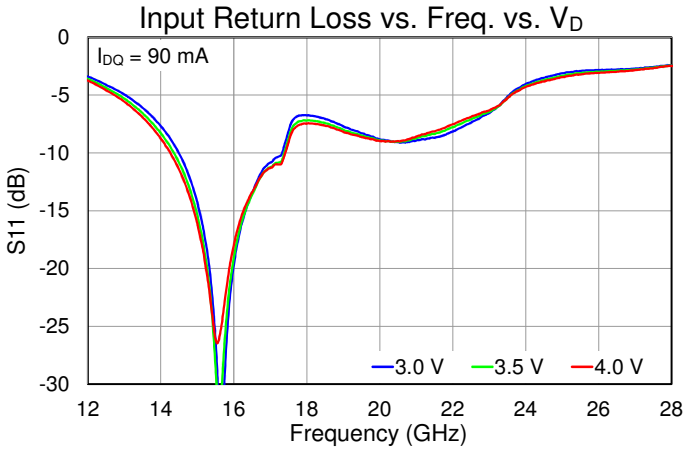
Gain vs. Frequency vs. V_D



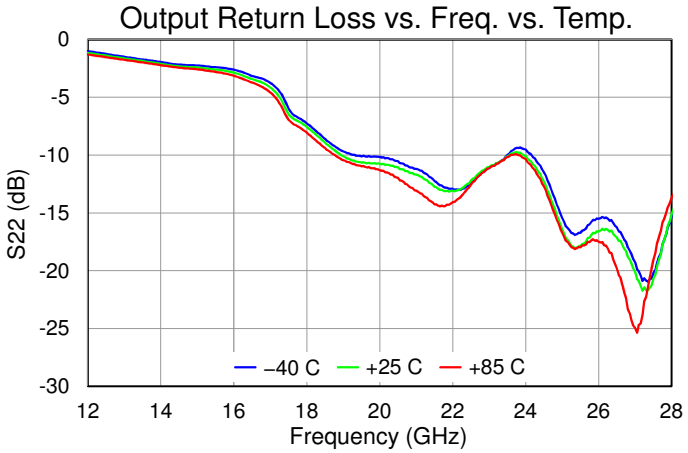
Input Return Loss vs. Freq. vs. Temp.



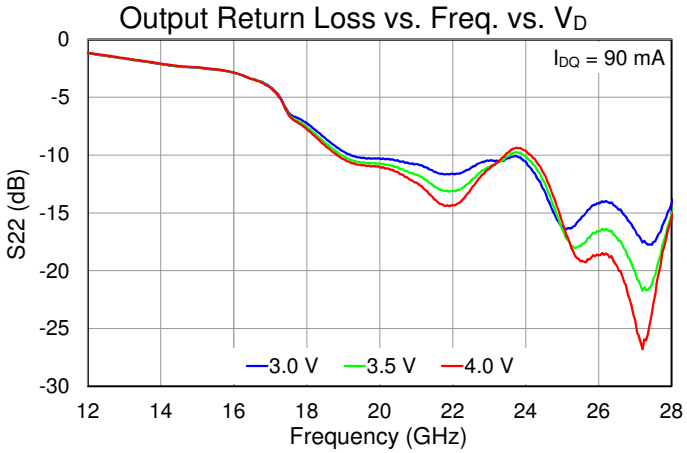
Input Return Loss vs. Freq. vs. V_D



Output Return Loss vs. Freq. vs. Temp.

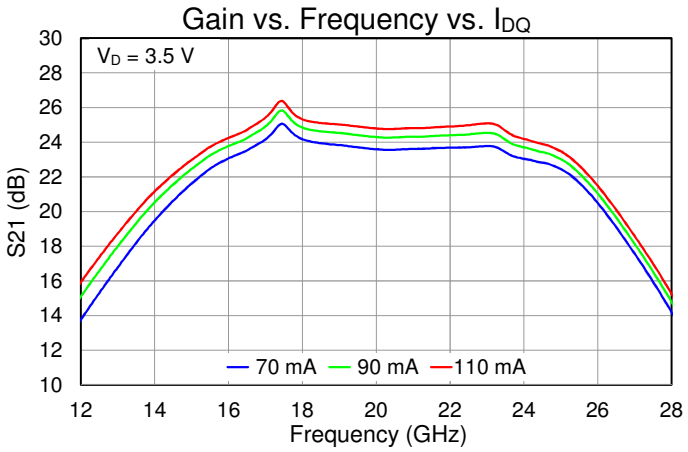


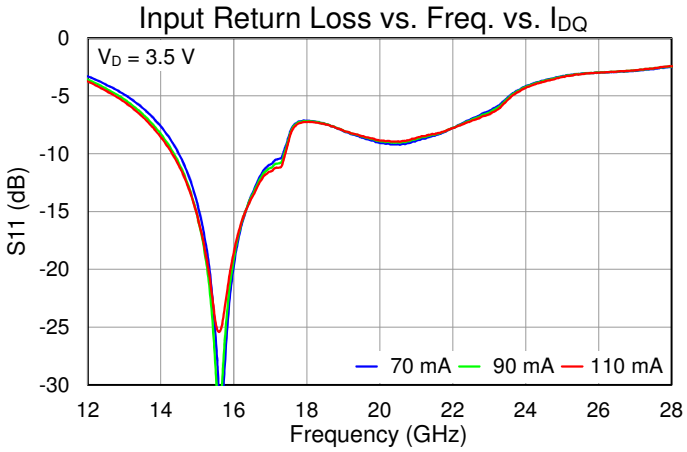
Output Return Loss vs. Freq. vs. V_D

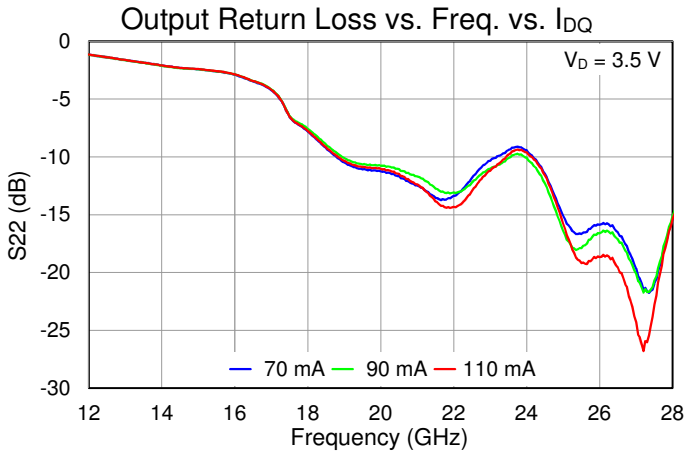


Performance Plots – Small Signal

Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C. Data de-embedded to MMIC bond wires.

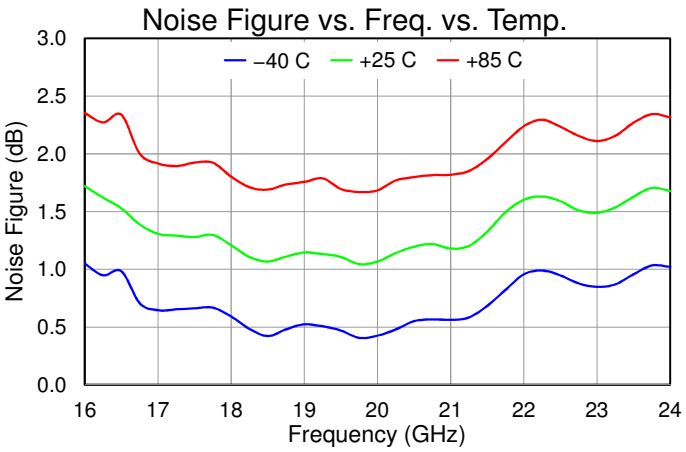


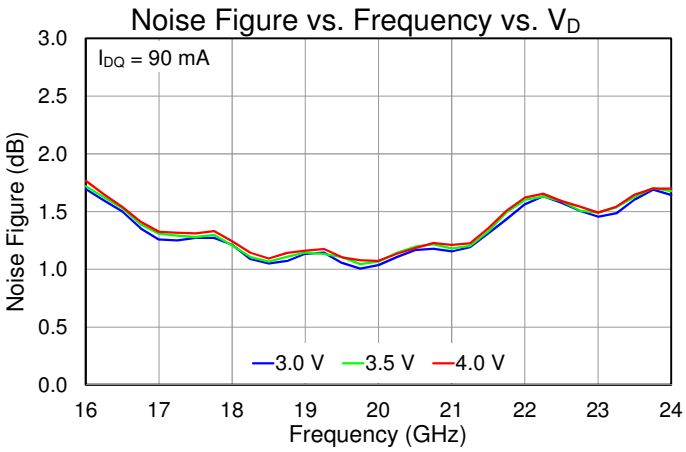


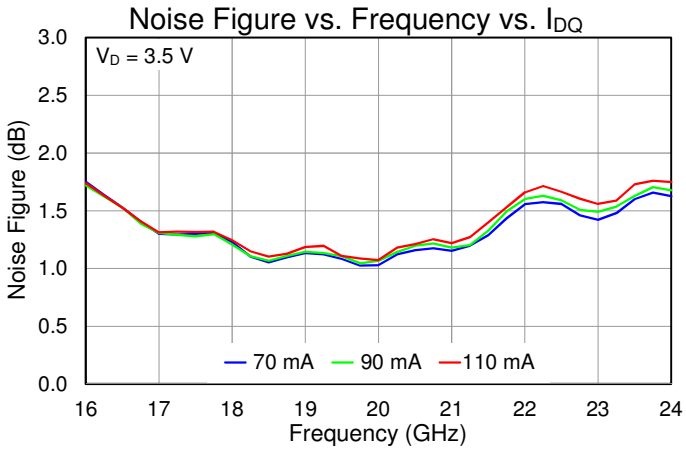


Performance Plots – Noise Figure

Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C. Data de-embedded to MMIC bond wires.



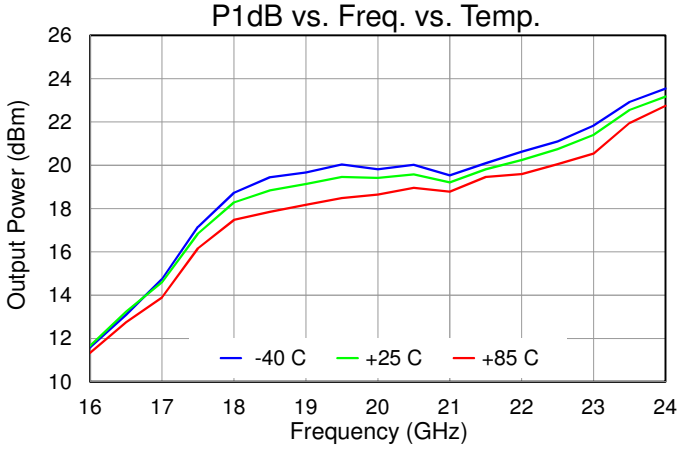




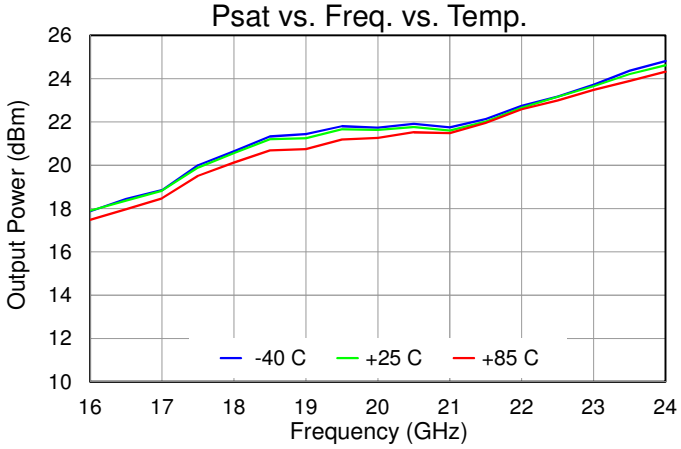
Performance Plots – Large Signal

Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C. Data de-embedded to MMIC bond wires.

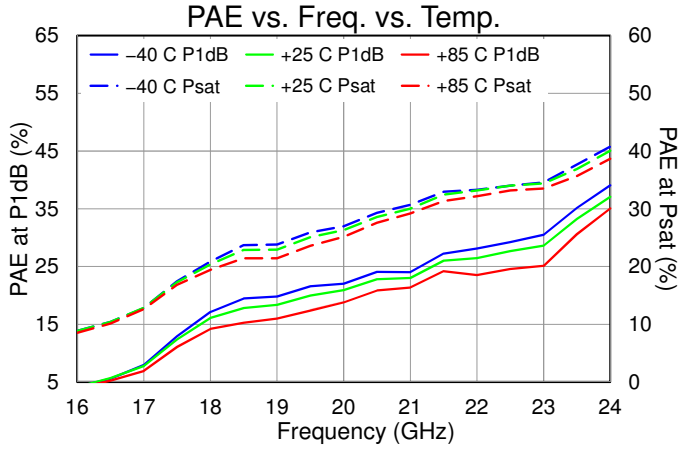
P1dB vs. Freq. vs. Temp.



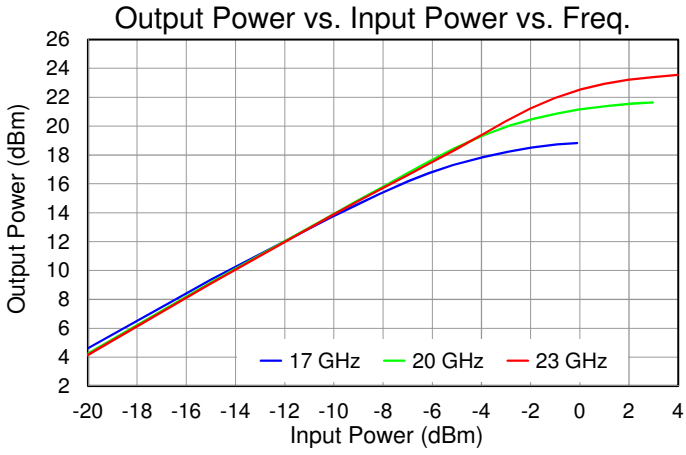
Psat vs. Freq. vs. Temp.



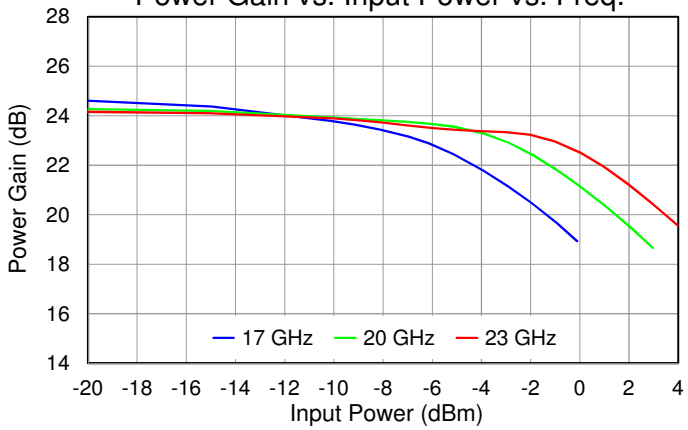
PAE vs. Freq. vs. Temp.



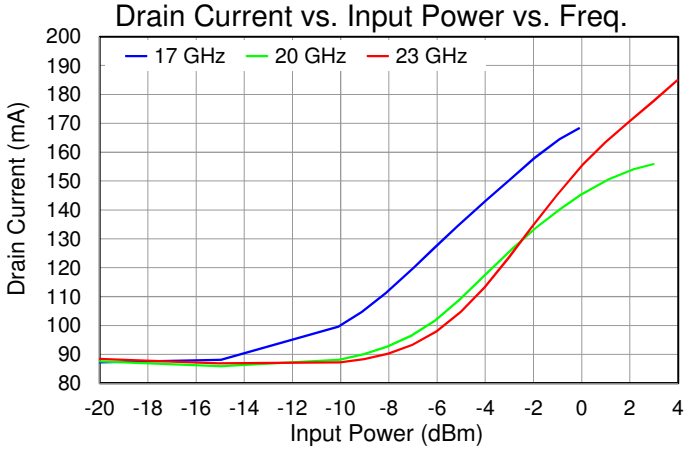
Output Power vs. Input Power vs. Freq.



Power Gain vs. Input Power vs. Freq.



Drain Current vs. Input Power vs. Freq.



Performance Plots – Linearity

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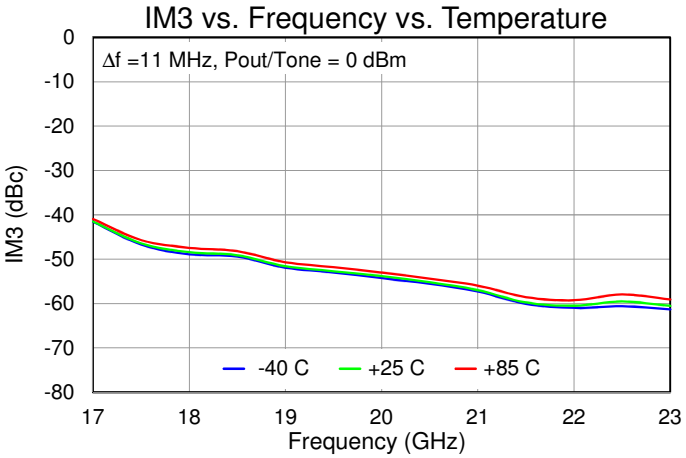

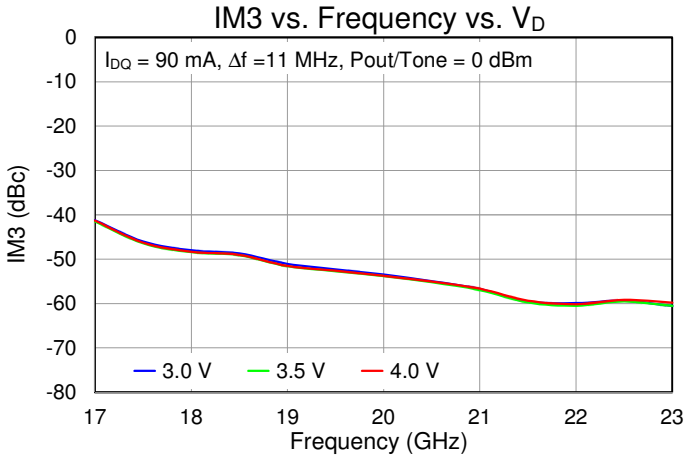

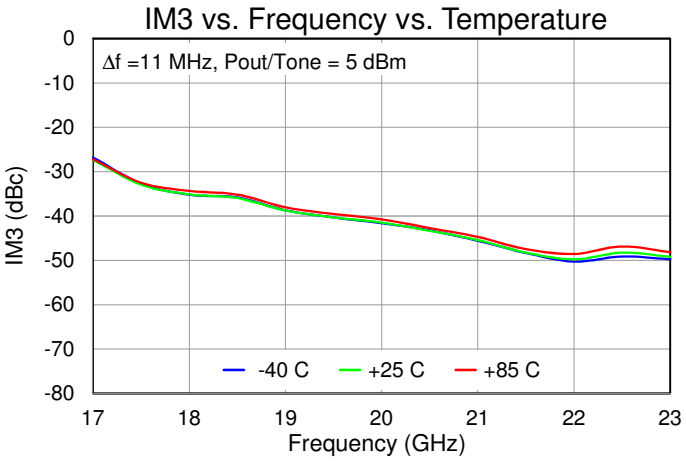

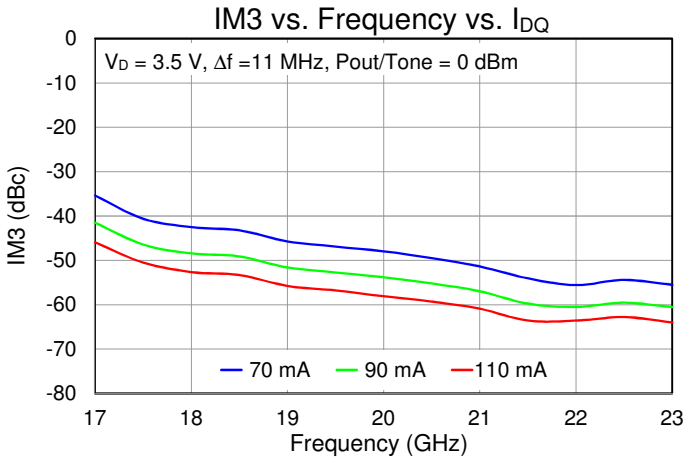

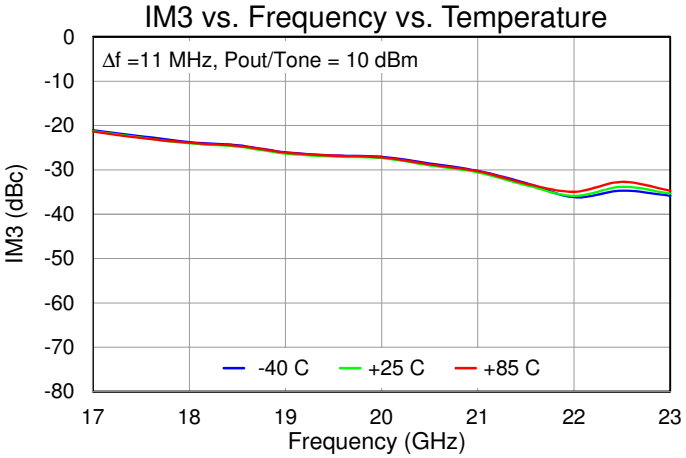

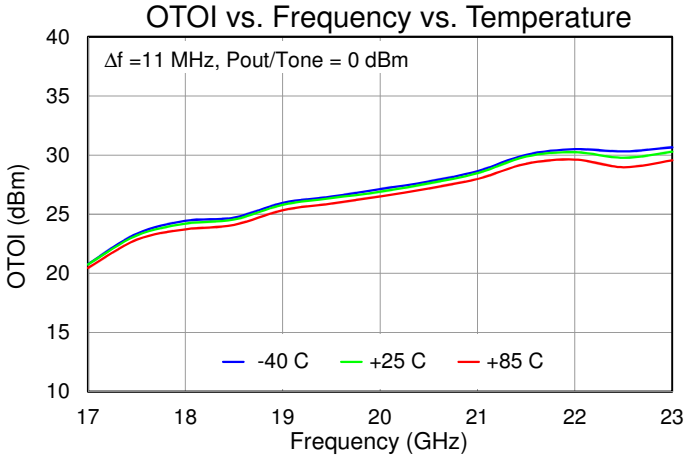

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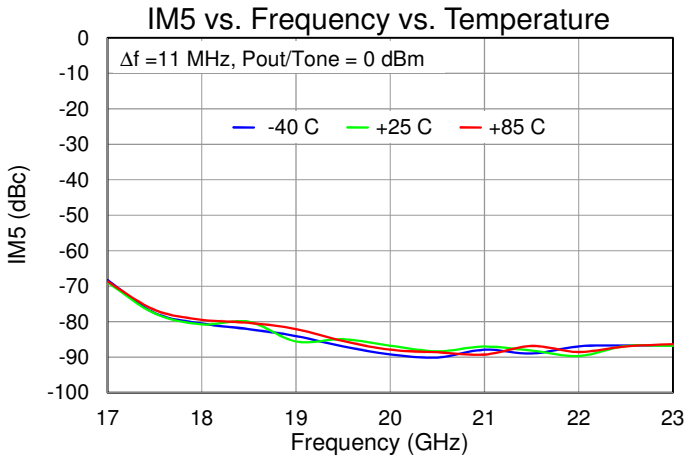
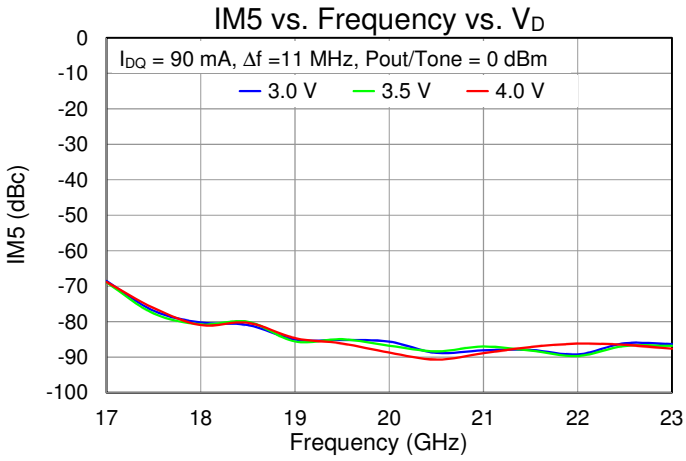
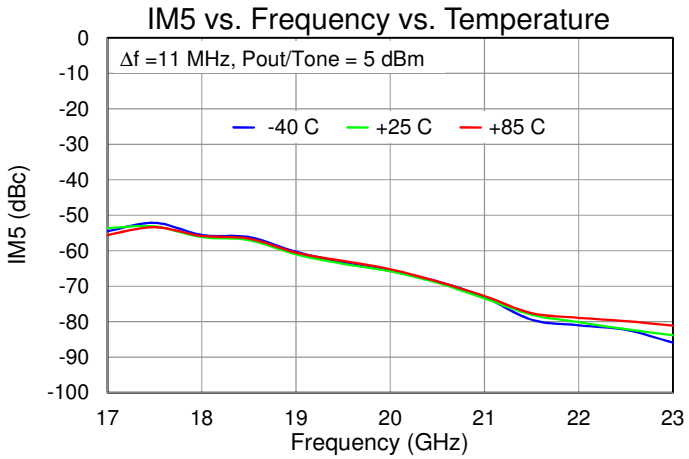
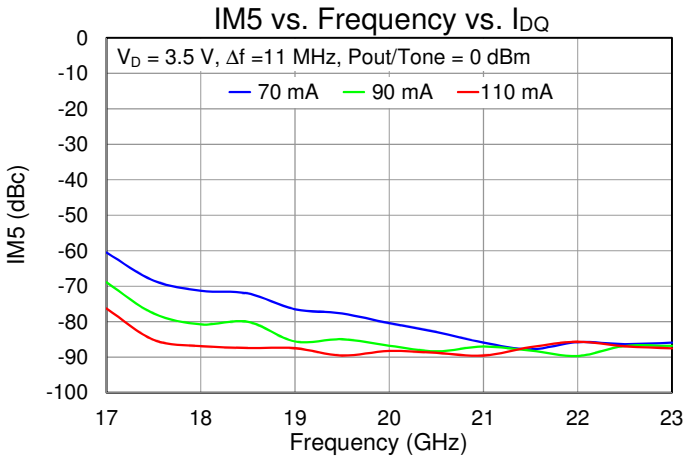
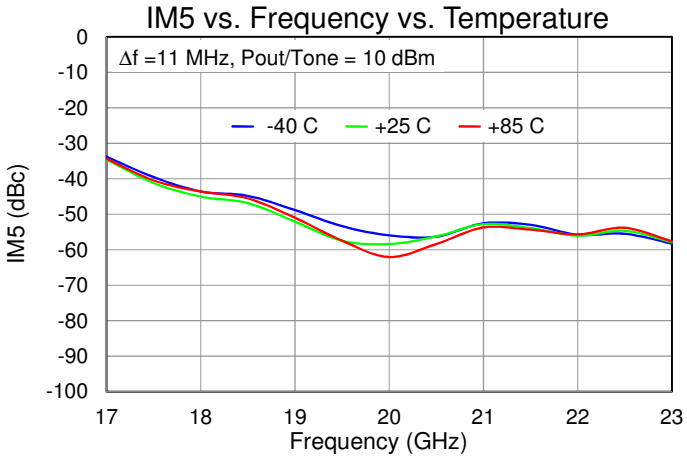










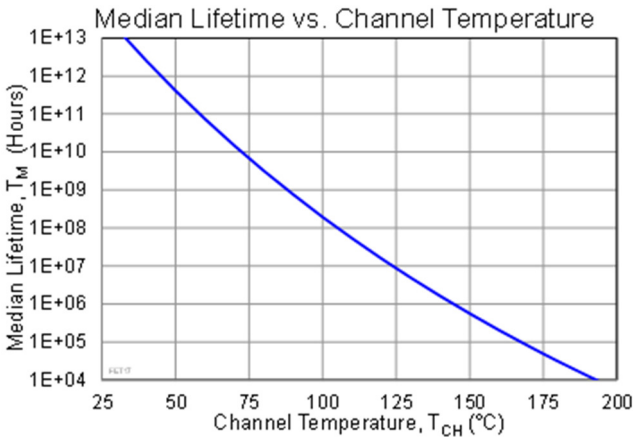
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 3.5 V, I_{DQ} = 90 mA Quiescent/Small Signal operation, P_{DISS} = 0.315 W	65.1	ºC/W
Channel Temperature, T_{CH} (Under RF)		105.5	°C
Median Lifetime (T_M)		1.226E08	Hrs

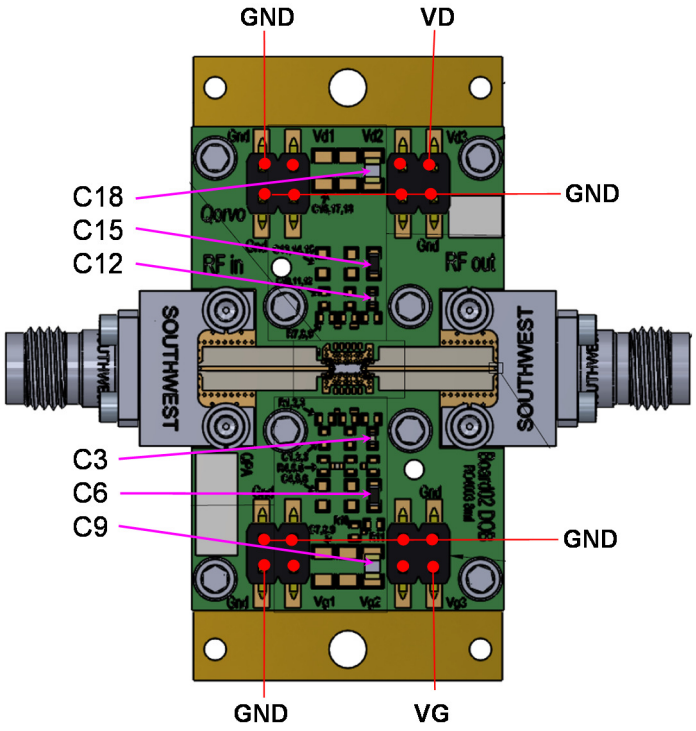
Notes:
1. Die mounted to 40 mil CuMo carrier plate with AuSn eutectic. Thermal resistance measured at back of carrier plate.

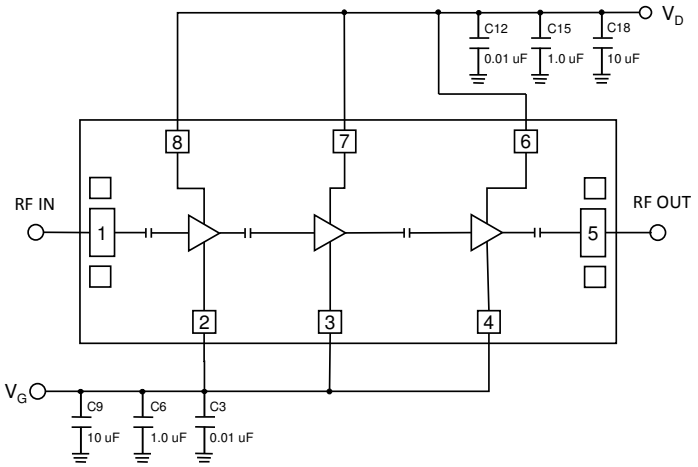
Median Lifetime

Test Conditions: V_D = +4 V
Failure Criteria is 10% reduction in I_{D_MAX}



Application Circuit and Evaluation Board Layout





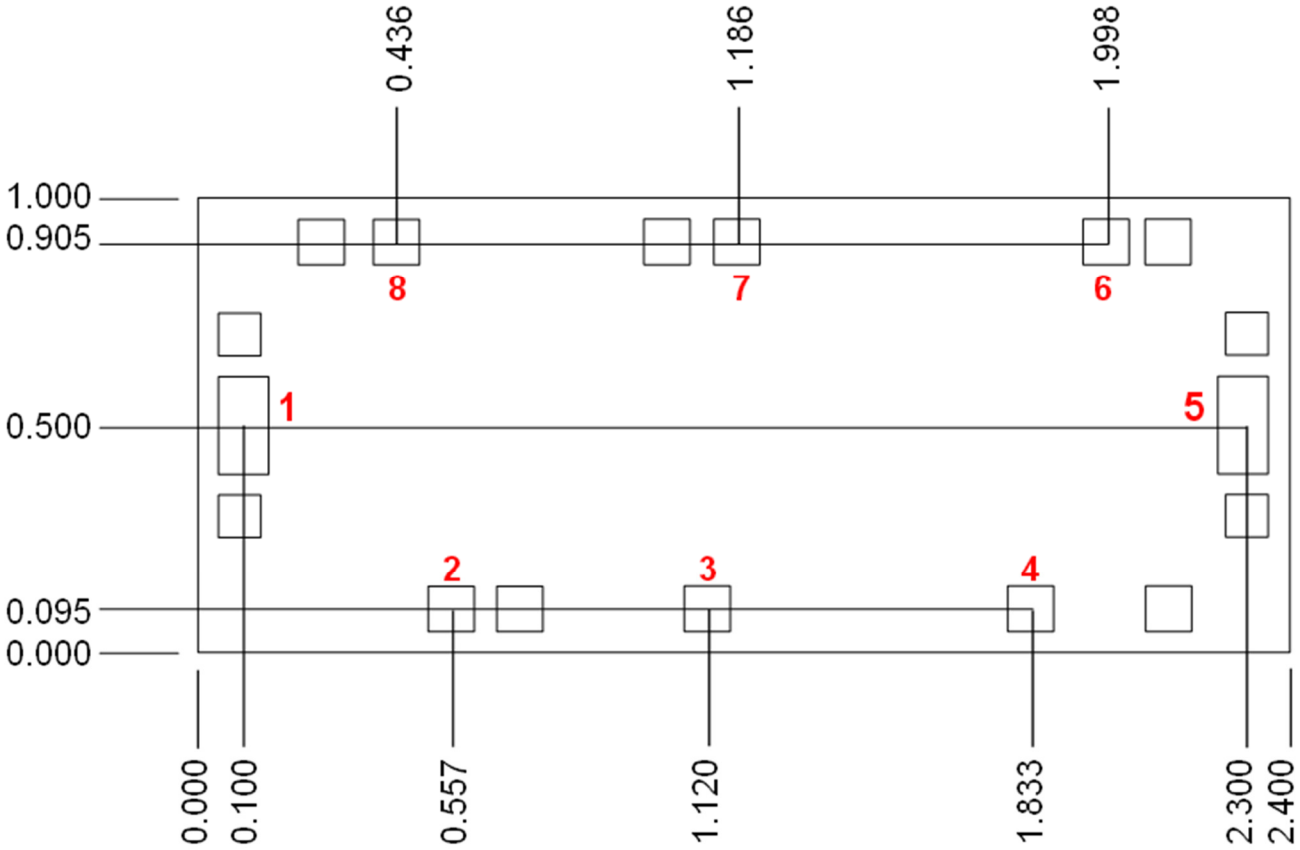
Notes:
1. See Evaluation Board PCB Information for material and stack up.

Bias-up Procedure	Bias-down Procedure
1. Set I_D limit to 220 mA, I_G limit to 10 mA	1. Turn off RF signal
2. Set V_G to –1.5 V	2. Reduce V_G to –1.5 V. Ensure $I_{DQ} \approx 0$mA
3. Set V_D +3.5 V	3. Set V_D to 0V
4. Adjust V_G more positive until I_{DQ} = 90mA ($V_G \approx$ –0.46 V Typical)	4. Turn off V_D supply
5. Apply RF signal	5. Turn off V_G supply

Bill of Material – Evaluation Board

Ref. Des.	Value	Description	Manuf.	Part Number
C3, C12	0.01 uF	CAP 0.01UF +/-10% 50V 0402 X7R ROHS	Various	
C6, C15	1.0 uF	CAP 1.0UF +/-10% 16V 0603 X7R ROHS	Various	
C9, C18	10 uF	CAP CER 10UF 10V X7R 10% 0805 TDK ROHS	Various	
RF IN, RF OUT	2.40 mm	2.40 MM END LAUNCH CONNECTOR	Southwest Microwave	1492-04A-5

Mechanical Drawing and Bond Pad Description



Dimensions in mm

Pad No.	Label	Description
1	RF Input	Matched to 50 ohms, DC blocked
2	VG1	Gate Voltage; bias network is required (VG can be tied together at PCB)
3	VG2	Gate Voltage; bias network is required (VG can be tied together at PCB)
4	VG3	Gate Voltage; bias network is required (VG can be tied together at PCB)
5	RF Output	Matched to 50 ohms, DC blocked
6	VD3	Drain Voltage; bias network is required (VD can be tied together at PCB)
7	VD2	Drain Voltage; bias network is required (VD can be tied together at PCB)
8	VD1	Drain Voltage; bias network is required (VD can be tied together at PCB)

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e., conductive epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

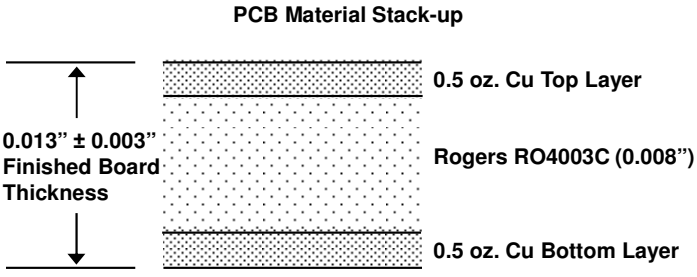
- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

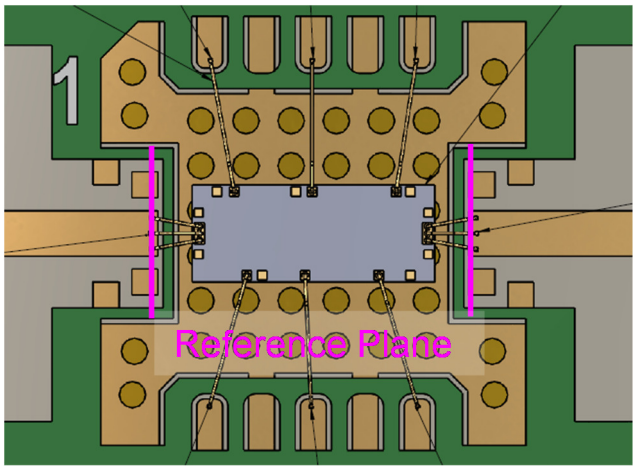
- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Evaluation Board PCB Information

Evaluation Board Stack-up



Die Mounting Detail



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ESDA / JEDEC JS-001-2012

Caution!
ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder and limit exposure to temperatures above 300 ℃ to 3-4 minutes, maximum.
Conductive epoxy die attach is recommended for PCB mounting.
Contact plating: Au

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

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