QPA2735

13.75 – 18 GHz GaAs Low Noise Amplifier

General Description

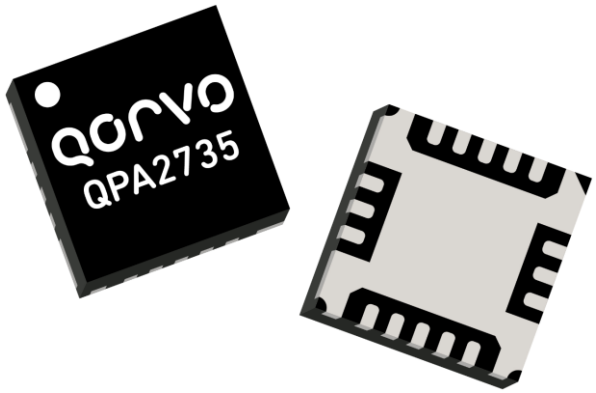
Qorvo's QPA2735 is a packaged, high-performance, low noise amplifier fabricated on Qorvo's production 90nm pHEMT (QPHT09) process. Covering 13.75 – 18 GHz, the QPA2735 provides 26 dB small signal gain and P1dB of 18 dBm, while supporting a noise figure of 1.1 dB and IM3 levels of −58 dBc (at Pout=0 dBm/tone).

Packaged in a small 4 mm x 4 mm plastic overmold QFN, the QPA2735 is matched to 50 ohms with integrated DC blocking caps on both I/O ports for easy handling and simple system integration.

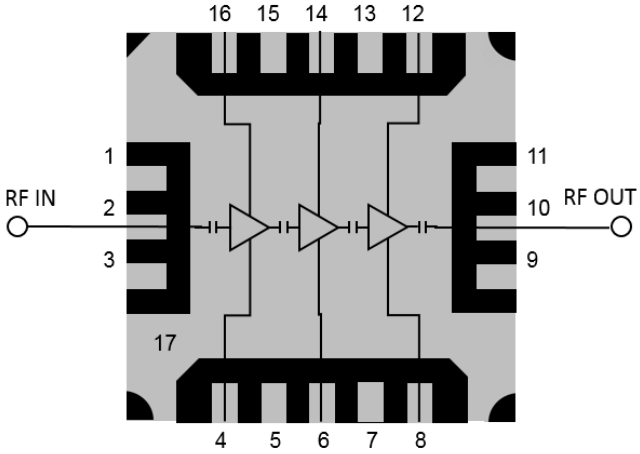
The QPA2735 high performance and ease of handling makes it ideal for satellite and point to point communication systems.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.



Functional Block Diagram



Product Features

- Frequency Range: 13.75 – 18 GHz
- Noise Figure: 1.1 dB
- Small Signal Gain: 26 dB
- P1dB: 18 dBm
- IMD3: −58 dBc (@ Pout=0 dBm/tone)
- Bias: V_D = 3.5 V, I_{DQ} = 105 mA, V_G = −0.46 V
- Plastic Overmold Package
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Performance is typical across frequency.
Please reference electrical specification table and data plots for more details.

Applications

- Satellite Communications
- Point to Point Communications

Ordering Information

Part No.	ECCN	Description
QPA2735S2	EAR99	QPA2735 Samples, Qty 2
QPA2735TR7X	EAR99	QPA2735 Tape and Reel, Qty 50
QPA2735TR7	EAR99	QPA2735 Tape and Reel, Qty 750
QPA2735EVBP1	EAR99	QPA2735 LNA Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	5.0 V
Drain Current ($I_{D1}/I_{D2}/I_{D3}$)	90/144/192 mA
Gate Voltage Range	0 to −1.5 V
Gate Current ($I_{G1}/I_{G2}/I_{G3}$ at 125 °C)	5.0/5.0/6.6 mA
RF Input Power (50 Ω, 85 °C)	20 dBm
Channel Temperature, T_{CH}	175 °C
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Recommended Operating Conditions

Parameter	Value
Drain Voltage	3.5 V
Drain Current (quiescent, I_{DQ})	105 mA
Gate Voltage (typical)	−0.46 V
Operating Temperature Range	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

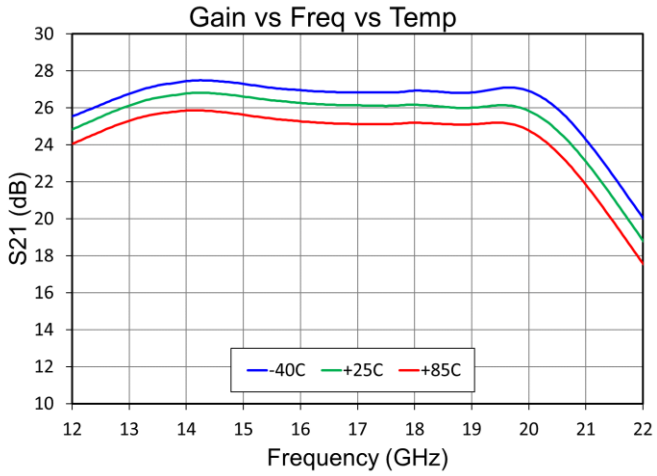
Electrical Specifications

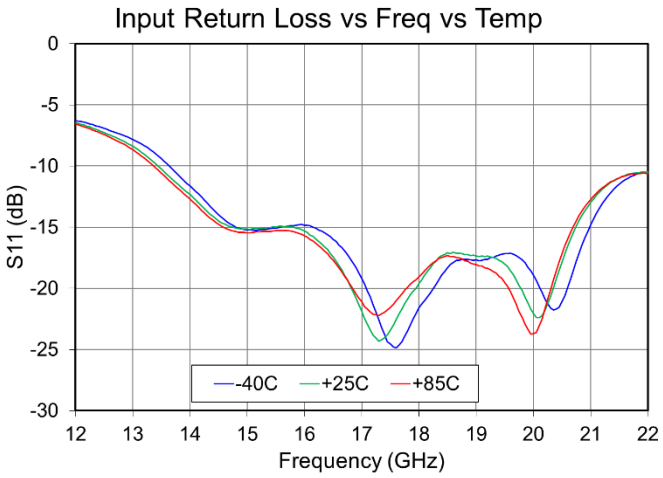
Test conditions, unless otherwise noted: 25 °C, V_D = 3.5 V, I_{DQ} = 105 mA. Data de-embedded to device reference plane.

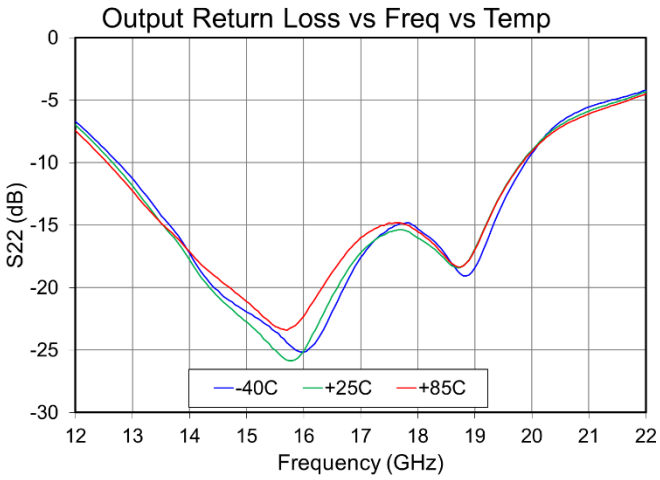
Parameter	Min	Typical	Max	Units
Frequency	13.75		18	GHz
Small Signal Gain		26		dB
Noise Figure		1.1		dB
1-dB Compression Point		18		dBm
Input Return Loss		11		dB
Output Return Loss		14		dB
3RD Order Intermodulation level (Pout=0 dBm / tone)		−58		dBc
Output TOI (Pout=0 dBm / tone)		29		dBm
Gain Temperature Coefficient		−0.013		dB/°C

Performance Plots – Small Signal

Test Conditions unless otherwise stated: VD = 3.5V, IDQ = 105mA. Data de-embedded to device reference plane



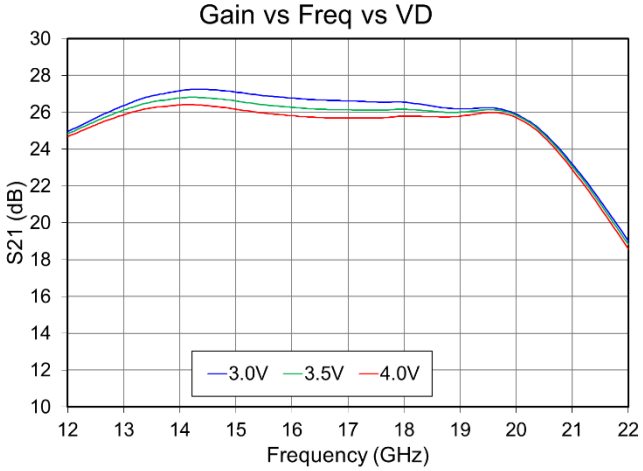




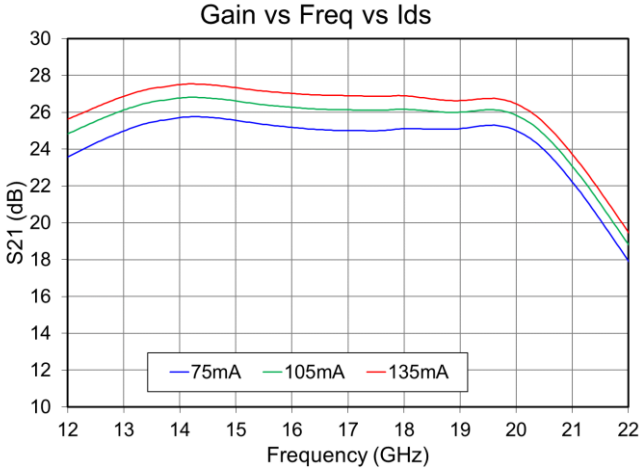
Performance Plots – Small Signal

Test Conditions unless otherwise stated: VD = 3.5V, IDQ = 105mA, 25C. Data de-embedded to the device reference

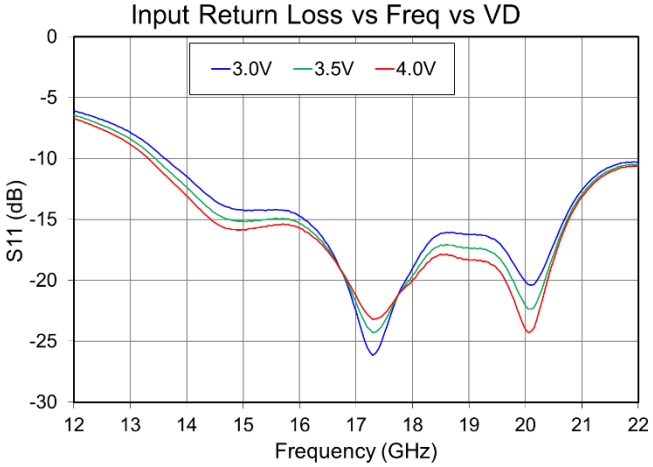
Gain vs Freq vs VD



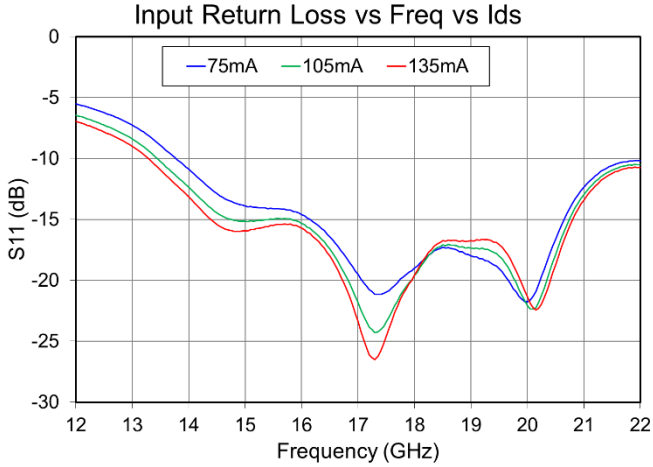
Gain vs Freq vs Ids



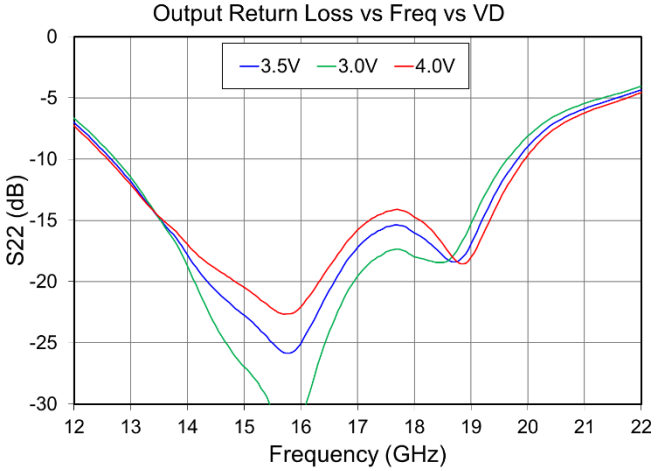
Input Return Loss vs Freq vs VD



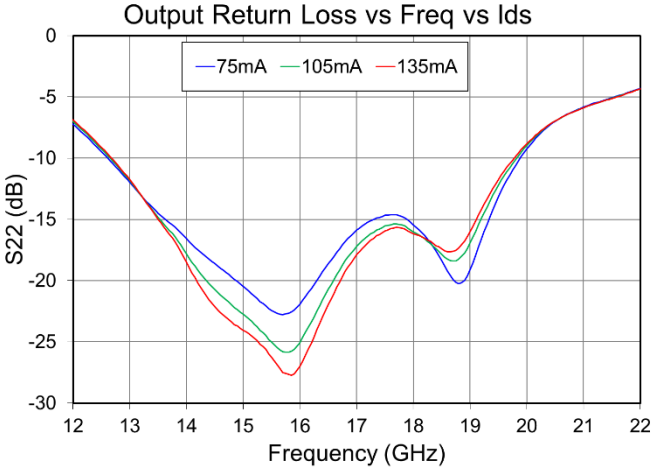
Input Return Loss vs Freq vs Ids



Output Return Loss vs Freq vs VD

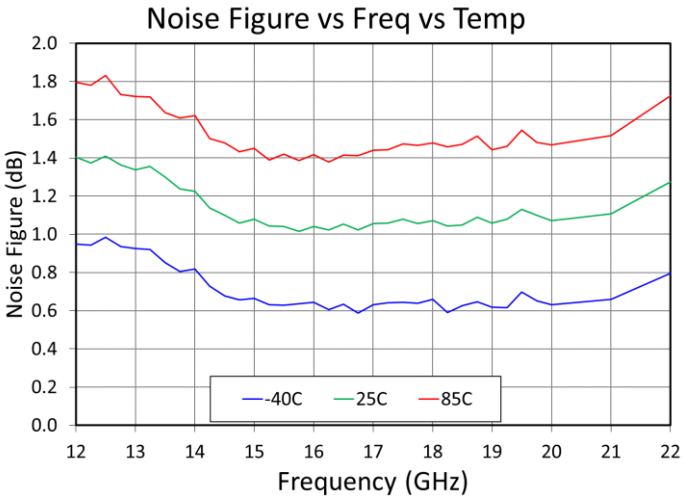


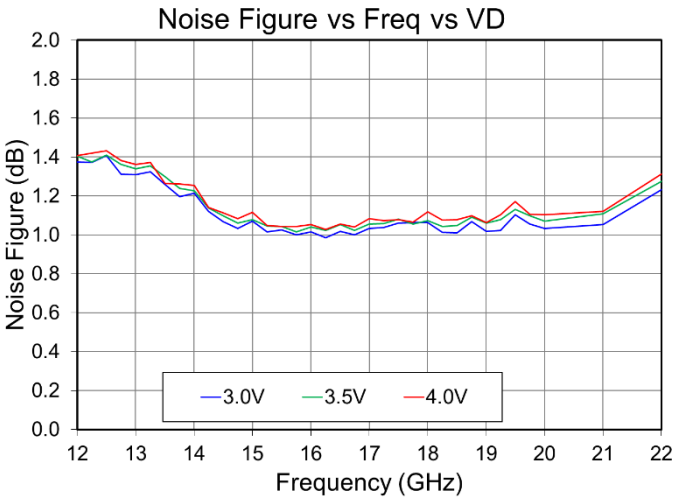
Output Return Loss vs Freq vs Ids

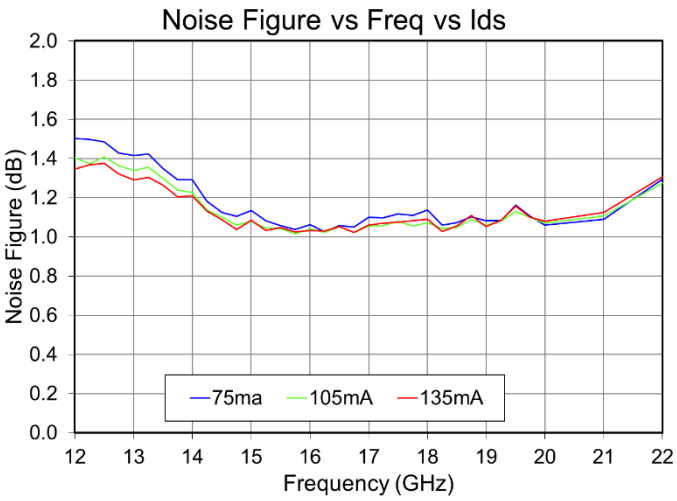


Performance Plots – Nose Figure

Test Conditions unless otherwise stated: VD = 3.5V, IDQ = 105mA, 25C. Data de-embedded to the device reference

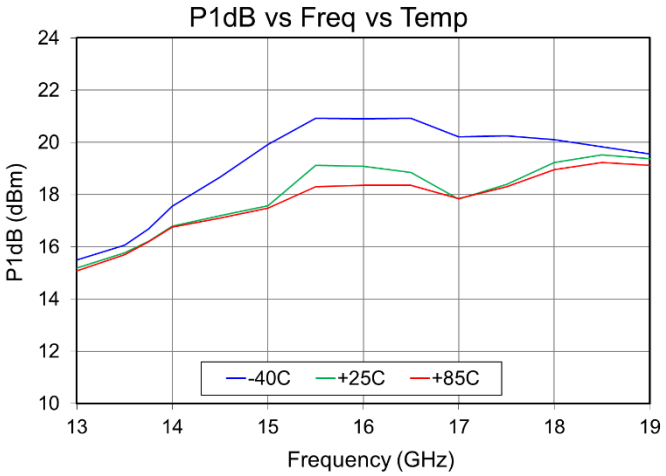


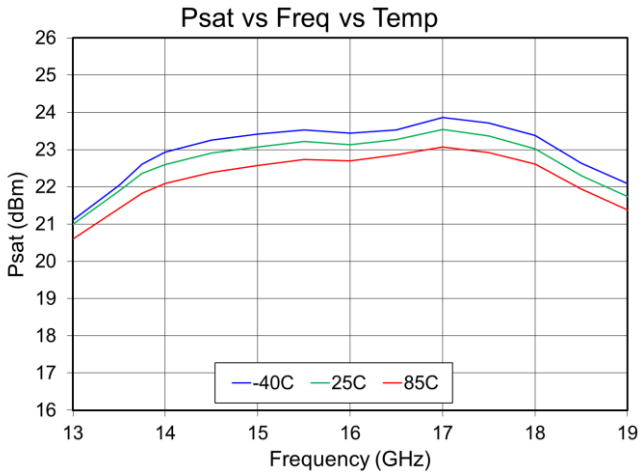


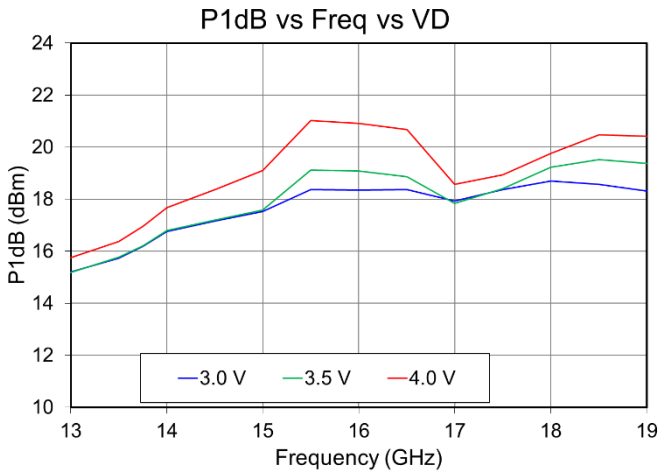


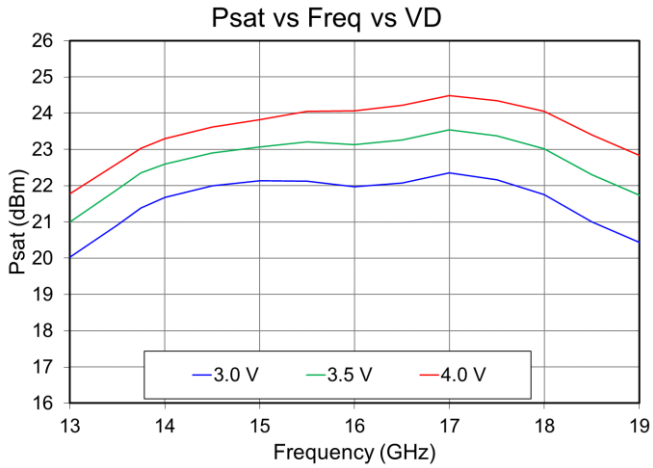
Performance Plots – Power

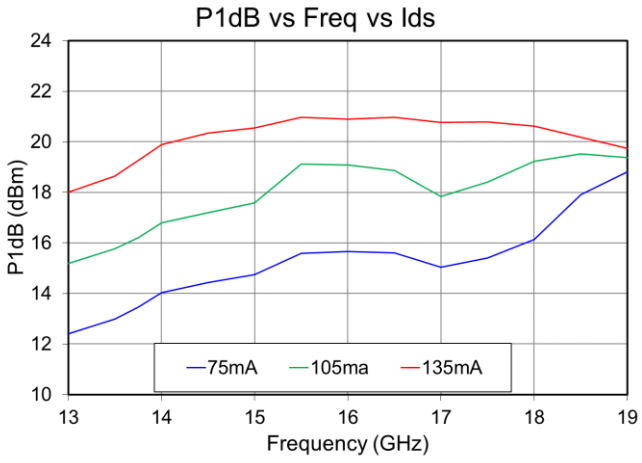
Test Conditions unless otherwise stated: VD = 3.5V, IDQ = 105mA, 25C. Data de-embedded to the device reference

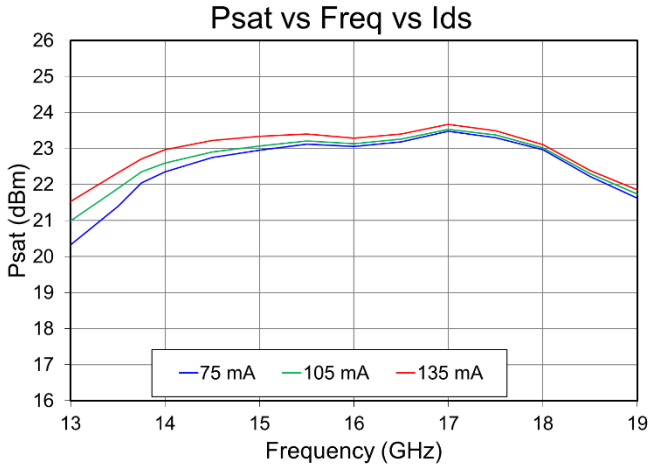






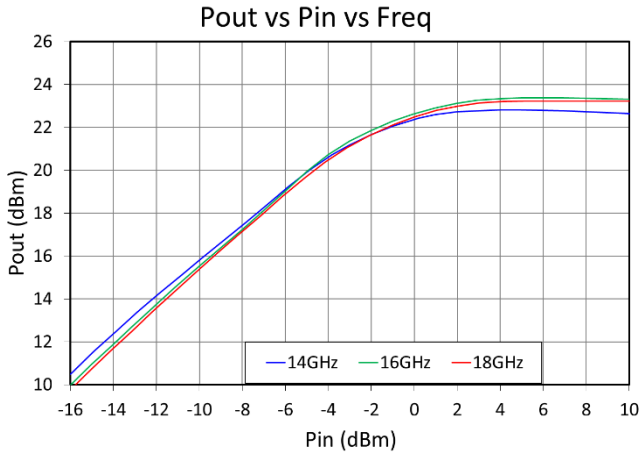


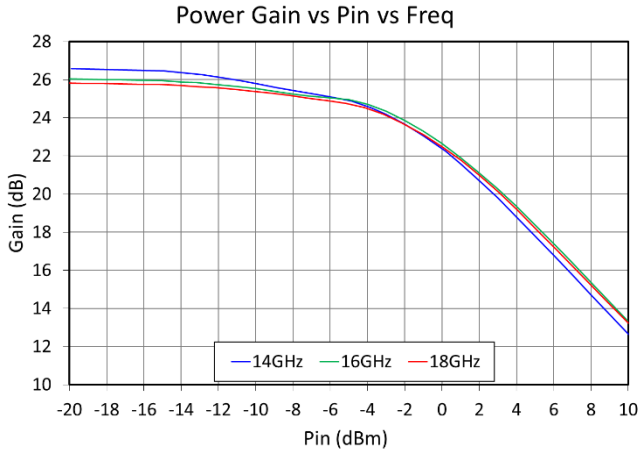


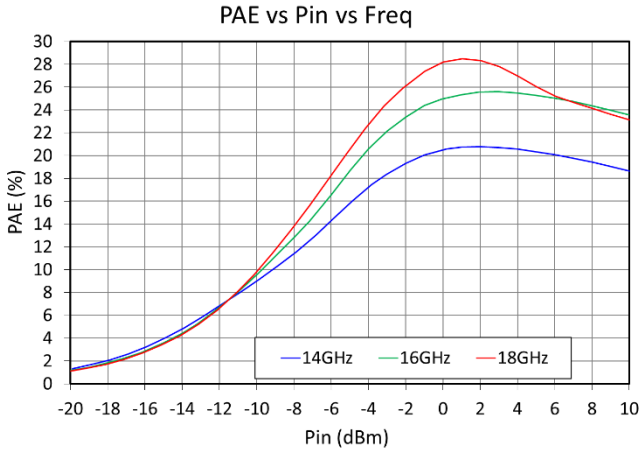


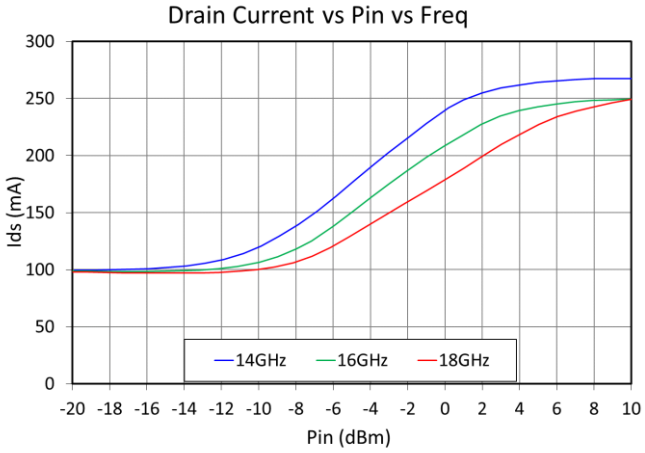
Performance Plots – Power Sweep

Test Conditions unless otherwise stated: VD = 3.5V, IDQ = 105mA, 25C. Data de-embedded to the device reference



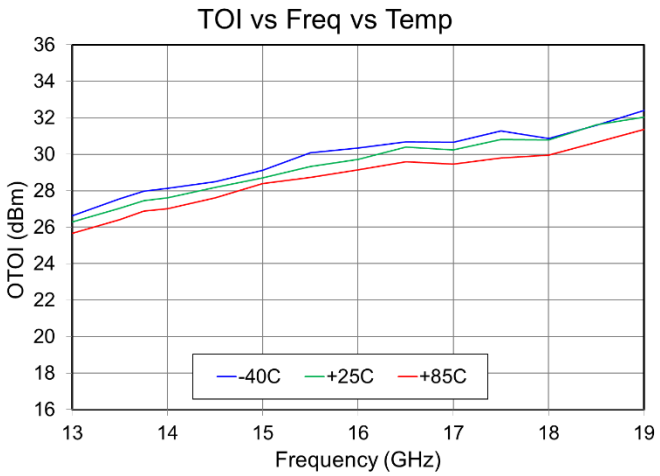


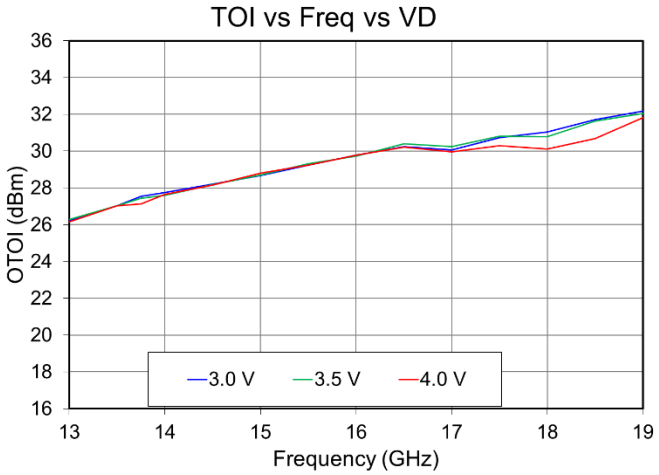


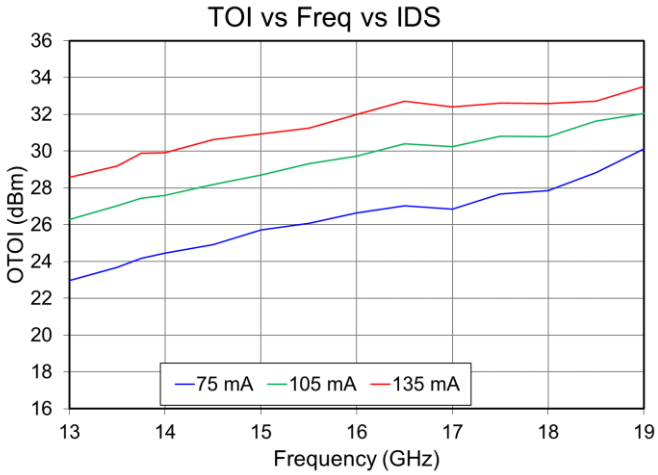


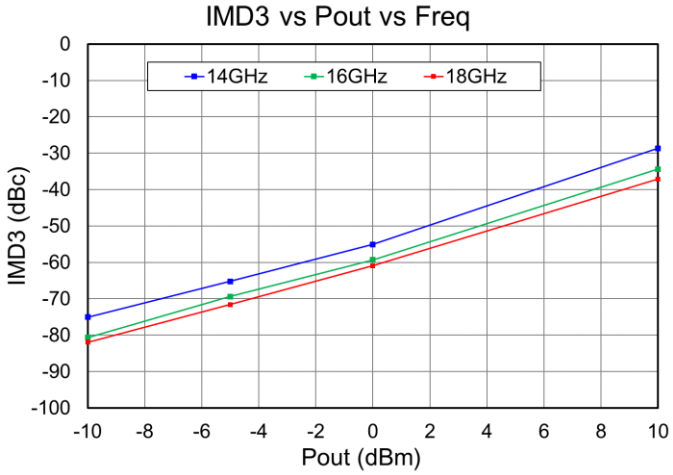
Performance Plots – Linearity

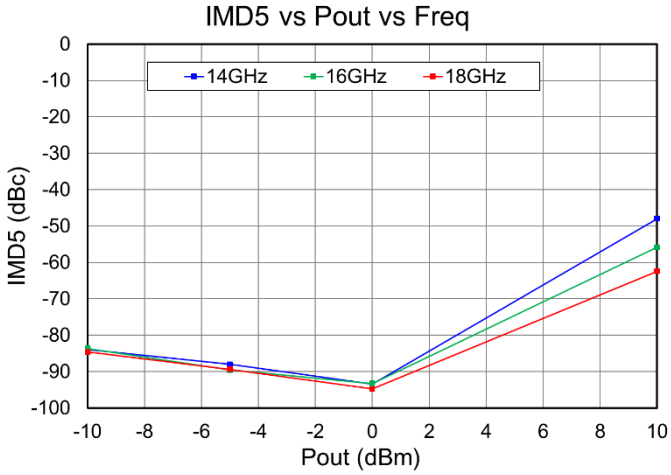
Test Conditions unless otherwise stated: VD = 3.5V, IDQ = 105mA, 25C. Data de-embedded to the device reference
Tone spacing 10MHz, Pout = -5dBm / tone



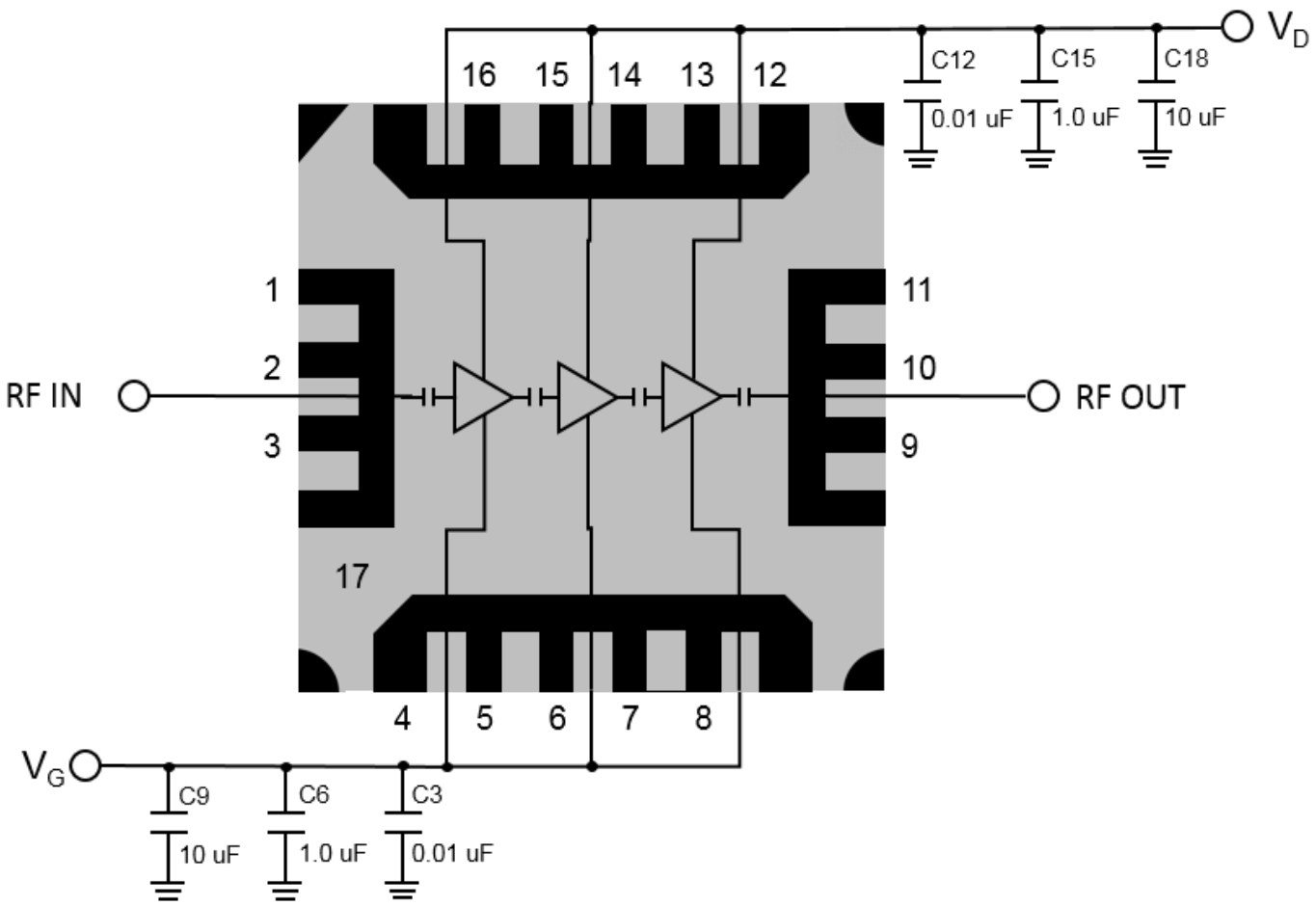








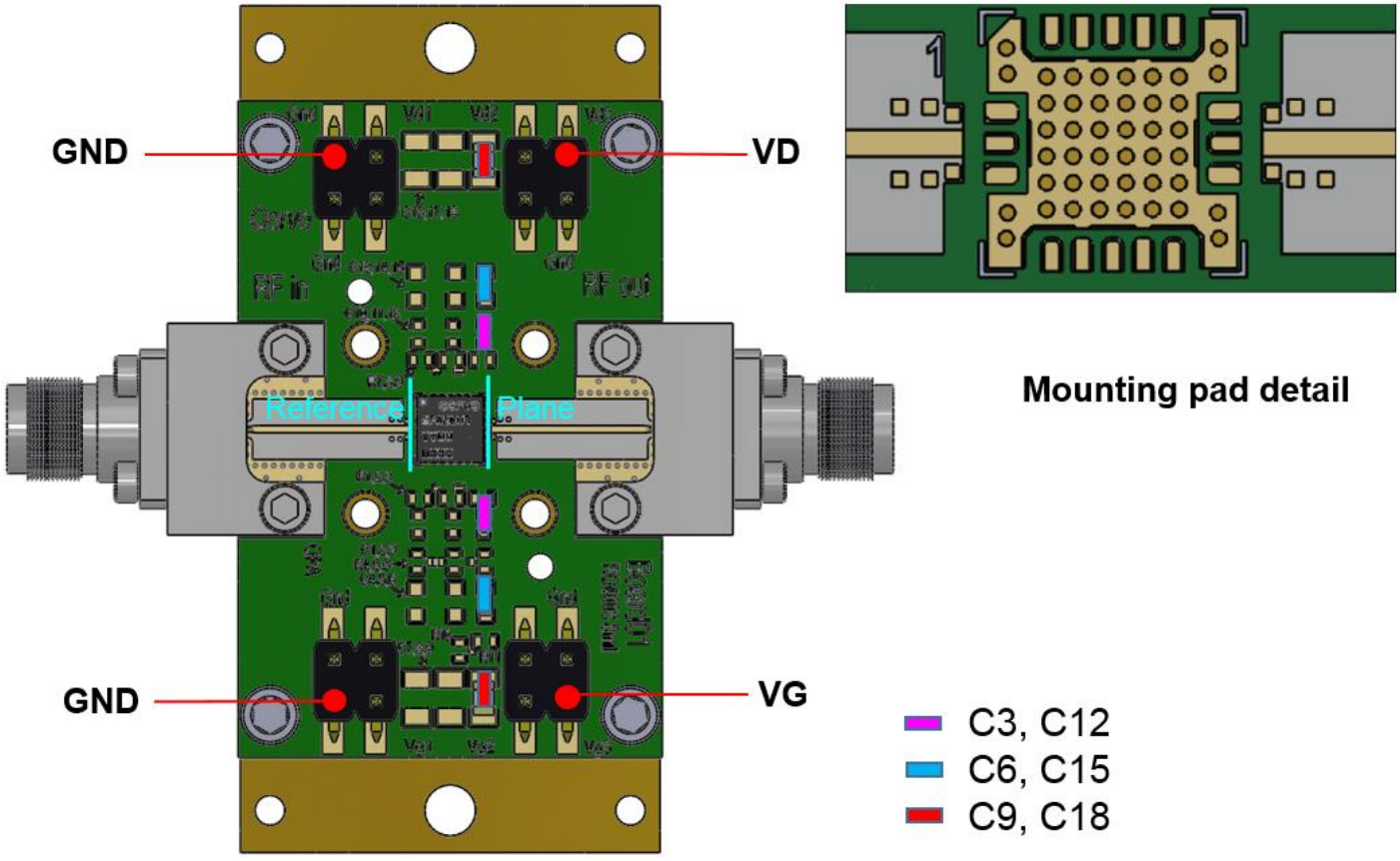
Application Circuit



Bias-up Procedure
1. Set I_D limit to 200 mA, I_G limit to 10 mA
2. Set V_G to −1.5 V
3. Set V_D +3.5 V
4. Adjust V_G more positive until I_{DQ} = 105mA (V_G ~ −0.46 V Typical)
5. Apply RF signal

Bias-down Procedure
1. Turn off RF signal
2. Reduce V_G to −1.5 V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board and Assembly



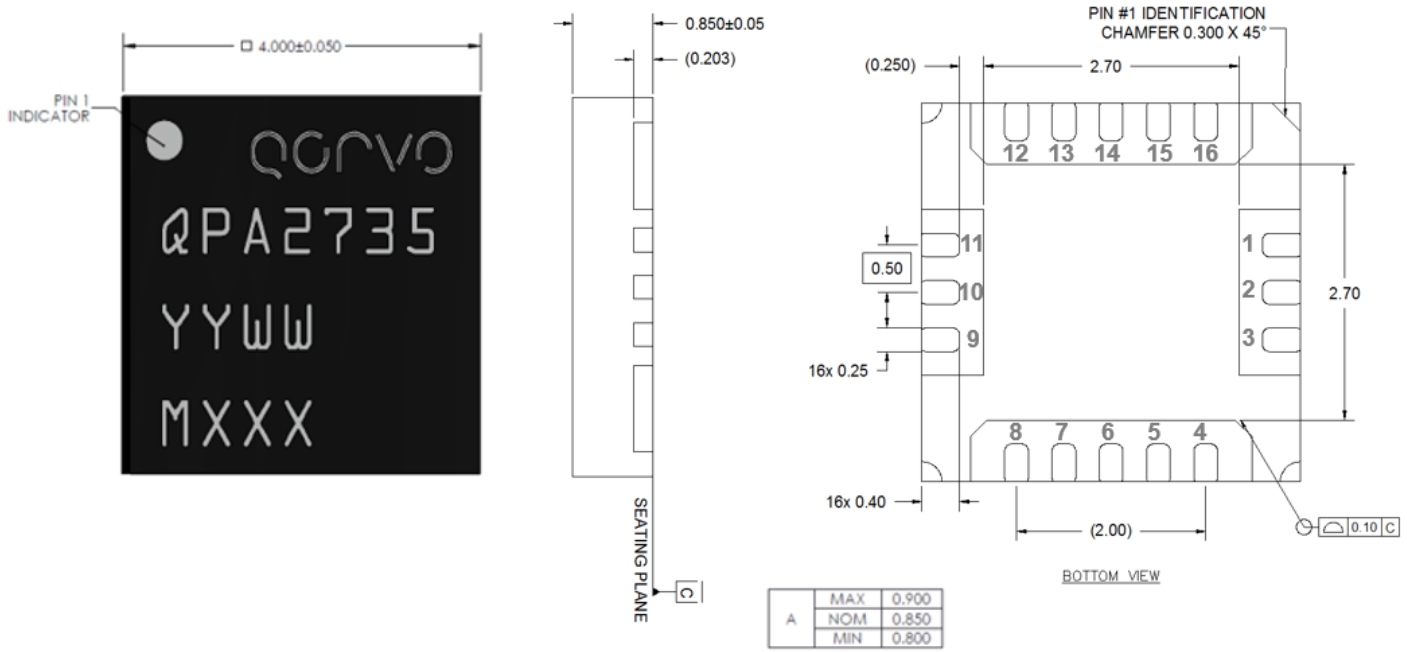
RF Layer is 0.008" thick Rogers Corp. RO4003C (ε_r = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.
The evaluation board PCB used the same design as that of QPA2626.

All data de-embedded to the device reference plane (shown).

Bill of Materials

Ref. Des.	Component	Value	Manuf.	Part Number
C3, C12	Surface Mount Cap.	CAP 0.01UF +/-10% 50V 0402 X7R ROHS	Various	
C6, C15	Surface Mount Cap.	CAP 1.0UF +/-10% 16V 0603 X7R ROHS	Various	
C9, C18	Surface Mount Cap.	CAP CER 10UF 10V X7R 10% 0805 TDK ROHS	Various	

Mechanical Drawing & Pad Description



Dimensions in mm
Part Marking:
2735: Part Number
YY = Part Assembly Year
WW = Part Assembly Week
MXXX = Batch ID

Pin Number	Label	Description
1, 3, 9, 11, 17 (slug)	**GND**	**GROUND**
2	RF Input	Matched to 50 ohms, DC blocked
4	VG1	Gate Voltage; bias network is required (V_G can be tied together at PCB)
6	VG2	Gate Voltage; bias network is required (V_G can be tied together at PCB)
8	VG3	Gate Voltage; bias network is required (V_G can be tied together at PCB)
10	RF Output	Matched to 50 ohms, DC blocked
12	VD3	Drain Voltage; bias network is required (V_D can be tied together at PCB)
14	VD2	Drain Voltage; bias network is required (V_D can be tied together at PCB)
16	VD1	Drain Voltage; bias network is required (V_D can be tied together at PCB)
5, 7, 13, 15	N/C	No internal connection. Recommend to GND at the PCB level

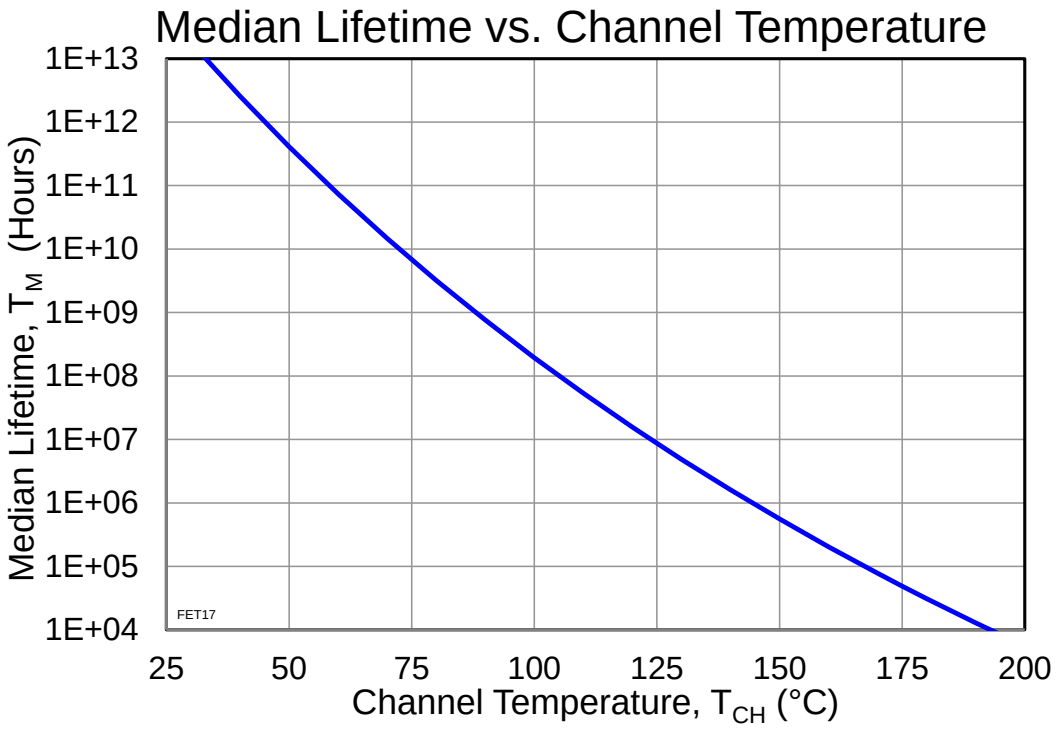
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 3.5 V, I_{DQ} = 105 mA Quiescent/Small Signal operation P_{DISS} = 0.3675 W	65.0	°C/W
Channel Temperature (T_{CH})		108.9	°C
Median Lifetime (T_M)		6.8E07	Hrs

Notes:
1. Thermal resistance is measured to back of the package.

Median Lifetime

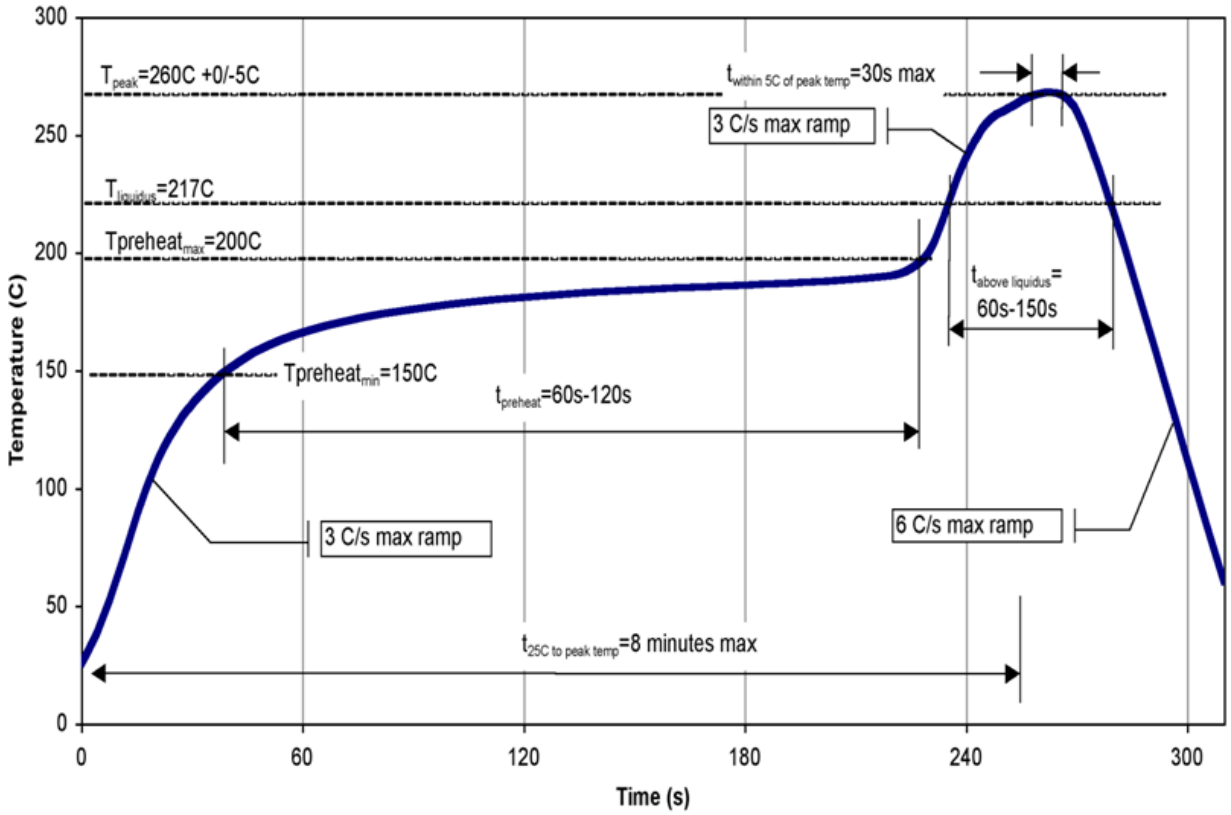
Test Conditions: V_D = 4 V
Failure Criteria = 10% reduction in I_{D_MAX}



Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	TBD	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	Level 3	JEDEC standard IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: www.qorvo.com

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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