

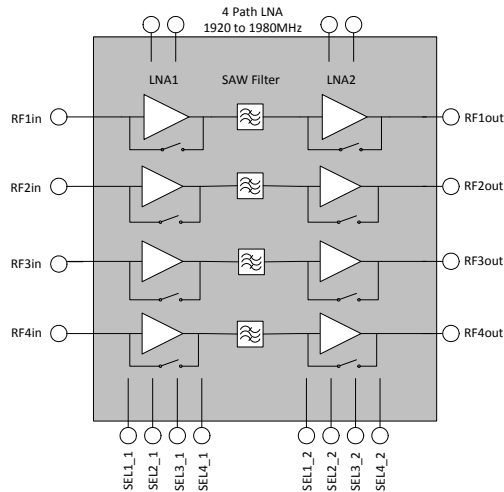


### Features

- Frequency Range 1920MHz to 1980MHz
- Full Internal 50Ω Matched
- Bypass Mode of LNA for High Dynamic Range
- Max Gain = 29dB
- Noise Figure of 1.5dB Typical
- High IIP3 = -10dBm
- Single +3V Supply

### Applications

- 3G, 4G Cellular Base Station
- MIMO LNA
- Remote Radio Head LNA
- Active Antenna LNA



Functional Block Diagram

### Product Description

RFMD's RFLA1010 is a four-path, low noise amplifier module with integrated RX band filter. Each LNA can be bypassed to provide higher dynamic range. The RFLA1010 has very low power consumption, with each LNA path drawing only 10mA from a 3V supply. It is packaged in a highly integrated 10mm x 10mm, multi-chip module (MCM) that is internally matched to 50Ω.

### Ordering Information

RFLA1010SR	7" Reel with 100 pieces
RFLA1010SQ	Sample Bag with 25 pieces
RFLA1010TR7	7" Reel with 500 pieces
RFLA1010TTR13	13" Reel with 1500 pieces
RFLA1010PCK-410	1920MHz to 1980MHz PCBA with 5-piece sample bag

### Optimum Technology Matching® Applied

<input type="checkbox"/> GaAs HBT	<input checked="" type="checkbox"/> SiGe BiCMOS	<input type="checkbox"/> GaAs pHEMT	<input type="checkbox"/> GaN HEMT
<input type="checkbox"/> GaAs MESFET	<input type="checkbox"/> Si BiCMOS	<input type="checkbox"/> Si CMOS	<input type="checkbox"/> BIFET HBT
<input type="checkbox"/> InGaP HBT	<input type="checkbox"/> SiGe HBT	<input type="checkbox"/> Si BJT	<input type="checkbox"/> LDMOS

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+3.6	V <sub>DC</sub>
Control Voltage	+3.6	V <sub>DC</sub>
DC Supply Current	50	mA
Power Dissipation	0.15	mW
Operating Temperature (T <sub>CASE</sub> )	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Junction Temperature (T <sub>J</sub> )	90	°C
ESD Rating - Human Body Model (HBM)	2000	V
Thermal Resistance	44.2	°C/W
Moisture Sensitivity Level	MSL3	



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

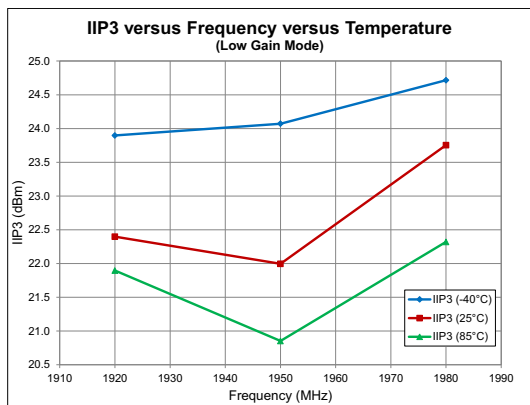
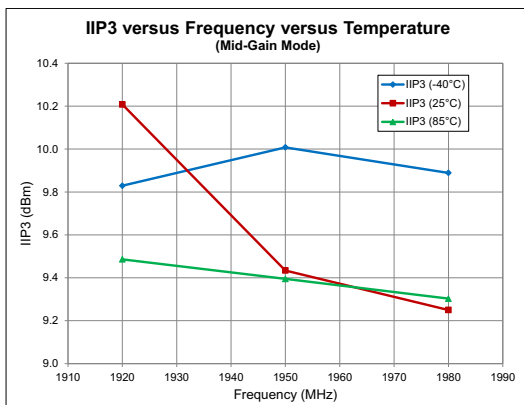
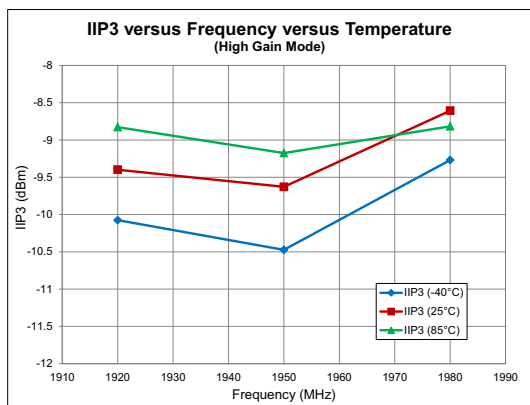
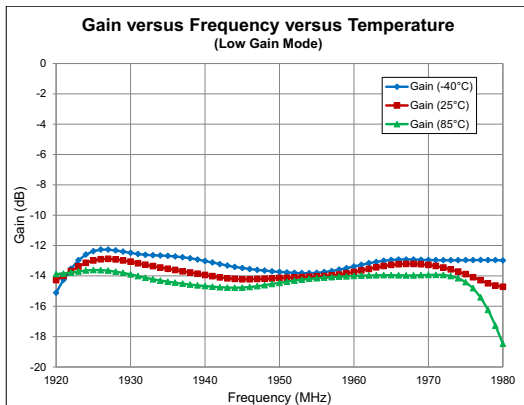
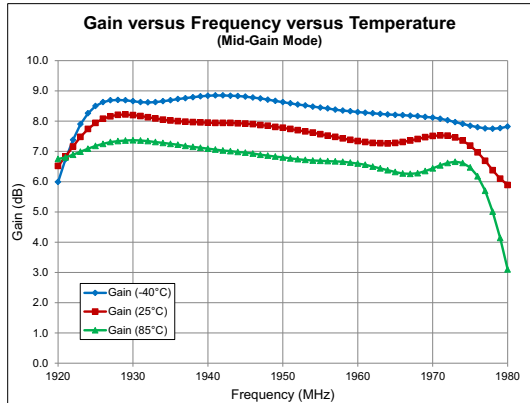
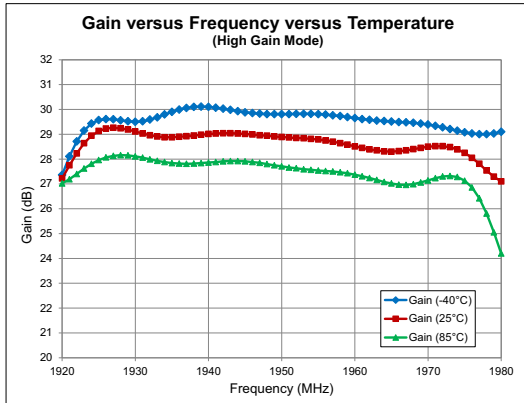
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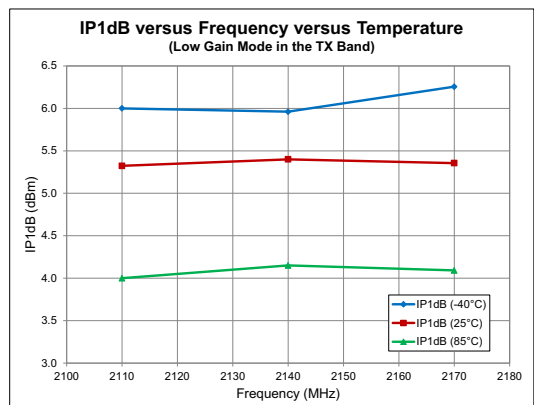
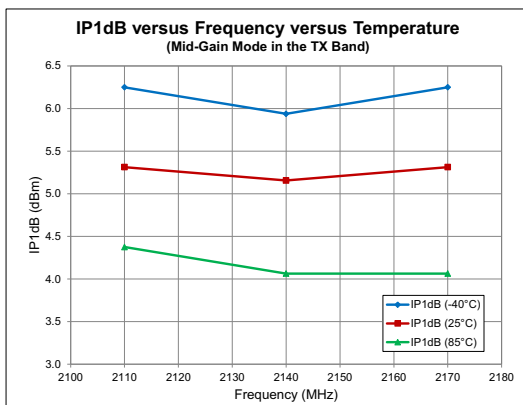
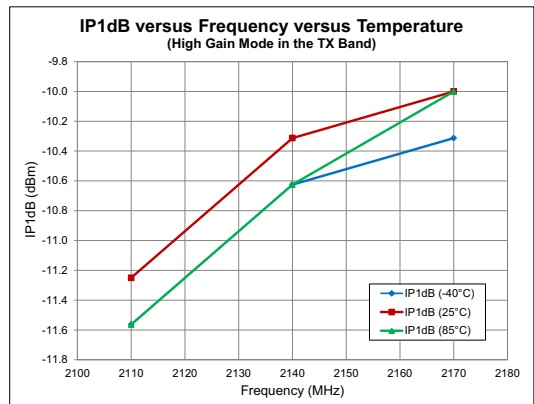
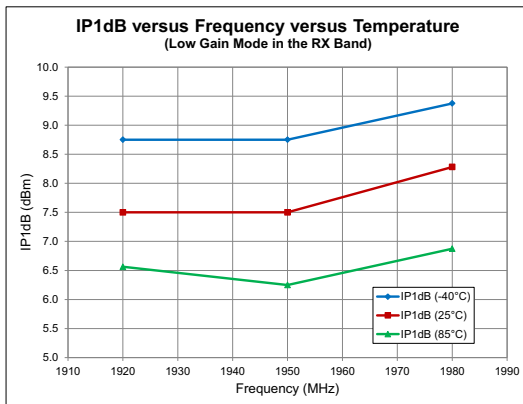
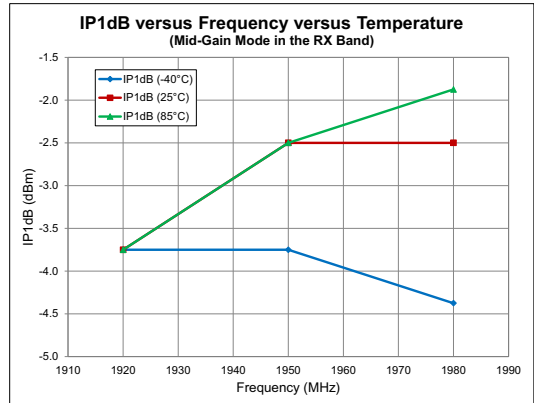
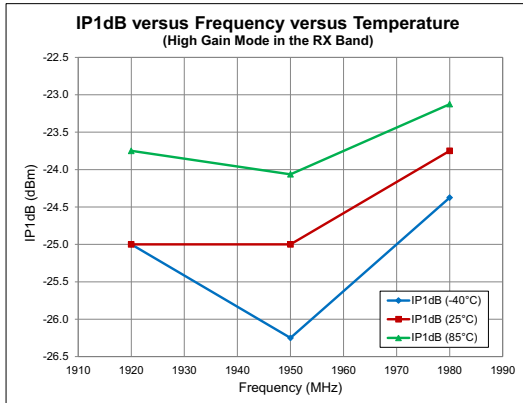


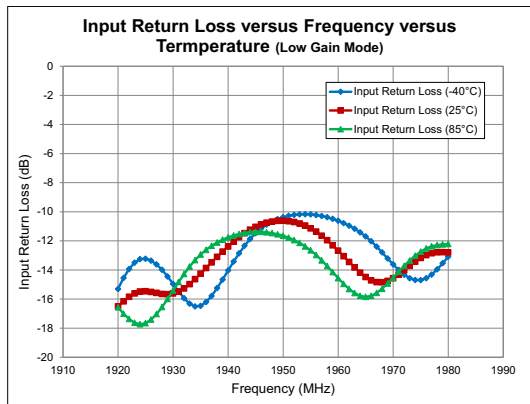
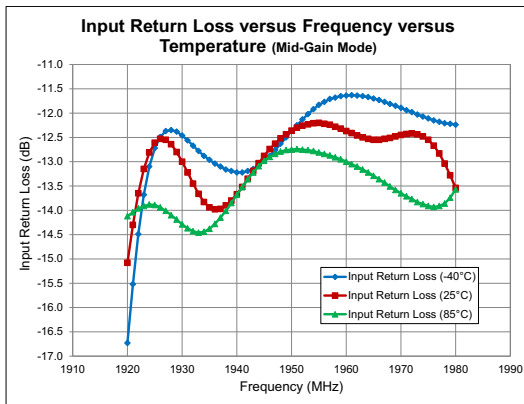
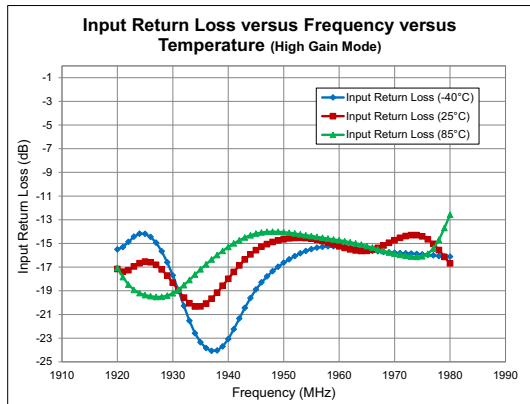
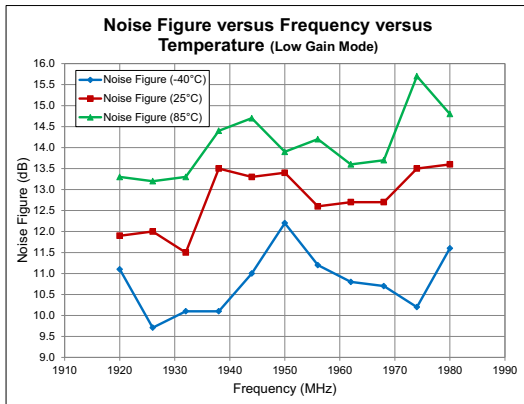
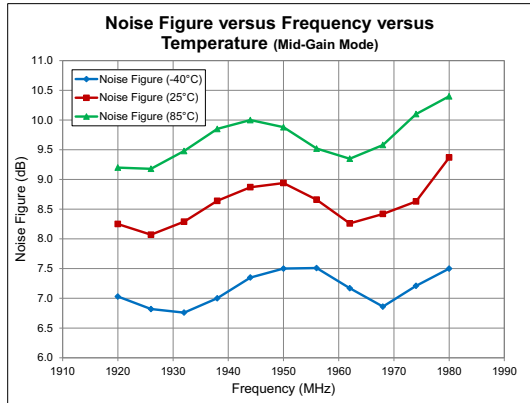
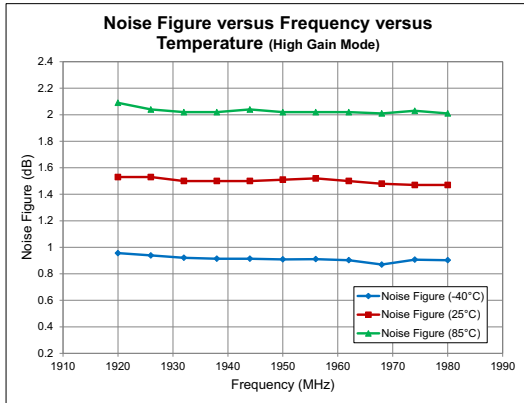
RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

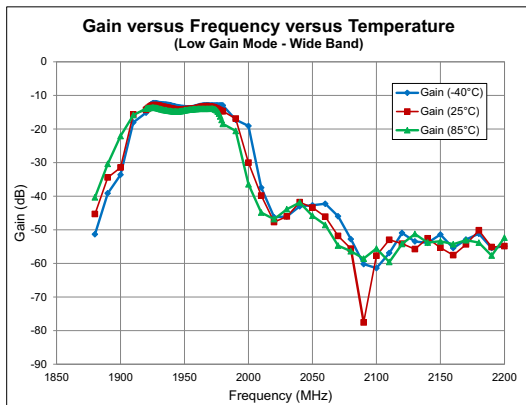
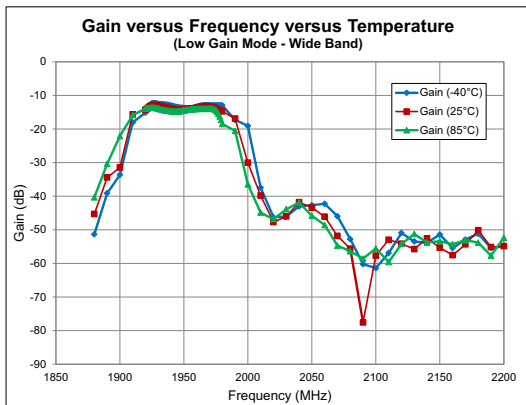
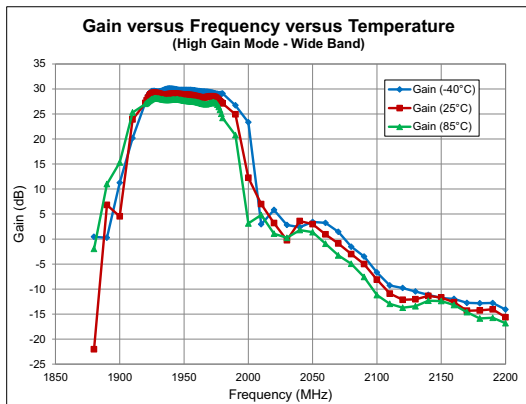
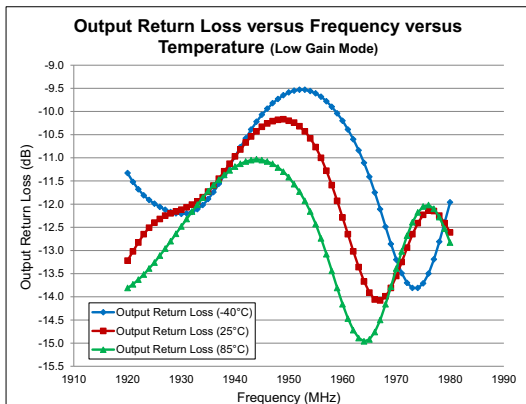
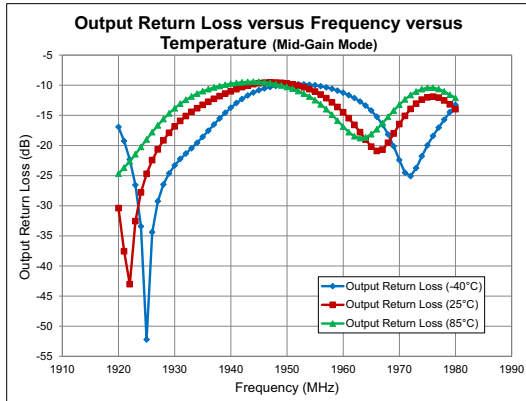
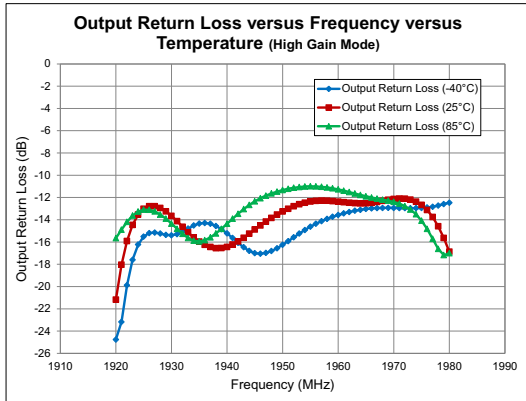
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>High Gain Mode Data</b>					Temp=25 °C, V <sub>CC</sub> =3V, Standard Application Circuit
Frequency Range	1920		1980	MHz	
Gain		28		dB	
Noise Figure		1.55		dB	
Input P1dB for RX In-band Signal		-21.5		dBm	
Input P1dB for TX Band Signal		-11		dBm	
IIP3 for RX In-band Signal (2 Tone Test)		-9		dBm	
Path to Path Isolation		-35		dB	
Current (Single LNA Path)		10.3		mA	
Input Return Loss		-15		dB	
Output Return Loss		-14.2		dB	
<b>Mid Gain Mode Data - First LNA Bypass</b>					Temp=25 °C, V <sub>CC</sub> =3V, Standard Application Circuit
Frequency Range	1920		1980	MHz	
Gain		7		dB	
Noise Figure		8.5		dB	
Input P1dB for RX In-band Signal		2.3		dBm	
Input P1dB for TX Band Signal		5		dBm	
IIP3 for RX In-band Signal (2 Tone Test)		9		dBm	
Current (Single LNA Path)		5		mA	
Input Return Loss		-11.6		dB	
Output Return Loss		-9.9		dB	
<b>Low Gain Mode Data - Both LNA Bypass</b>					Temp=25 °C, V <sub>CC</sub> =3V, Standard Application Circuit
Frequency Range	1920		1980	MHz	
Gain		-13.5		dB	
Noise Figure		12.3		dB	
Input P1dB for RX In-band Signal		8		dBm	
Input P1dB for TX Band Signal		5		dBm	
IIP3 for RX In-band Signal (2 Tone Test)		23		dBm	
Input Return Loss		-10.2		dB	
Output Return Loss		-10.2		dB	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					Temp = 25 °C, V <sub>CC</sub> = 3V, Standard Application Circuit
Supply Voltage	2.8	3	3.3	V	
Logic High (Select Control Lines)	1.8			V	
Logic Low (Select Control Lines)			0.8	V	
Total Current (HG Mode, 4 Paths)		42		mA	
Total Current (MG Mode, 4 Paths)		20		mA	
Total Current (LG Mode, 4 Paths)		<500		μA	









## Pin Names and Description Table

Pin	Function	Description
2	RFIN	RF Input (Internally 50Ω Matched)
4	SEL1_1	Switch Control Line
6	RF2_IN	RF Input (Internally 50Ω Match)
8	SEL2_1	Switch Control Line
12	RF3_IN	RF Input (Internally 50Ω Match)
14	SEL3_1	Switch Control Line
16	RF4_IN	RF Input (Internally 50Ω Match)
22	SEL4_1	Switch Control Line
27	VCC4	VCC Supply
31	SEL4_2	Switch Control Line
36	RF4_OUT	RF Output (Internally 50Ω Match)
38	SEL3_2	Switch Control Line
40	RF3_OUT	RF Output (Internally 50Ω Match)
42	VCC3	VCC Supply
44	SEL2_2	Switch Control Line
46	RF2_OUT	RF Output (Internally 50Ω Match)
48	SEL1_2	Switch Control Line
50	RF1_OUT	RF Output (Internally 50Ω Match)
56	VCC2	VCC Supply
59	VCC1	VCC Supply
All Other Pins	GND	Low Inductive Path to Ground

## Truth Table

SEL1_1	SEL1_2	SEL2_1	SEL2_2	SEL3_1	SEL3_2	SEL4_1	SEL4_2	
1	1	0	0	0	0	0	0	Path 1 High Gain
0	1	0	0	0	0	0	0	Path 1 Mid Gain
0	0	1	1	0	0	0	0	Path 2 High Gain
0	0	0	1	0	0	0	0	Path 2 Mid Gain
0	0	0	0	1	1	0	0	Path 3 High Gain
0	0	0	0	0	1	0	0	Path 3 Mid Gain
0	0	0	0	0	0	1	1	Path 4 High Gain
0	0	0	0	0	0	0	1	Path 4 Mid Gain
0	0	0	0	0	0	0	0	All Paths Low Gain

Note: All control lines are independent. More than one path could be on at the same time.



Dimensions in millimeters

Technical drawing of a square plate, showing three views: Top View, Side View, and Bottom View.

**Top View:** A square plate with overall dimensions  $10.000 \pm 0.10$  mm. A circular feature is located in the top-left corner. The center point is labeled 'C'. The thickness of the plate is indicated as  $0.440$  mm.

**Side View:** Shows the thickness of the plate as  $1.340 \pm 0.04$  mm. The center point 'C' is also indicated.

**Bottom View:** A detailed view of the plate's bottom surface, showing a grid of holes. The holes are arranged in a  $17 \times 17$  pattern. The center point is labeled 'C'. The dimensions of the holes and the plate are as follows:

- Overall dimensions:  $10.000 \pm 0.10$  mm (Top View)
- Thickness:  $0.440$  mm (Side View)
- Center point: 'C' (indicated in all views)
- Hole dimensions:  $0.100$  mm (All Edges)
- Hole spacing:  $34 \times 0.350$  mm (indicated in the grid)
- Hole spacing:  $34 \times 0.363$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 4.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 3.500$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 3.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 2.500$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 2.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 1.500$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 1.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 0.500$  mm (indicated in the grid)
- Hole dimensions:  $0.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 4.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 3.500$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 3.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 2.500$  mm (indicated in the grid)
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- Hole dimensions:  $2 \times 1.500$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 1.000$  mm (indicated in the grid)
- Hole dimensions:  $2 \times 0.500$  mm (indicated in the grid)
- Hole dimensions:  $0.000$  mm (indicated in the grid)

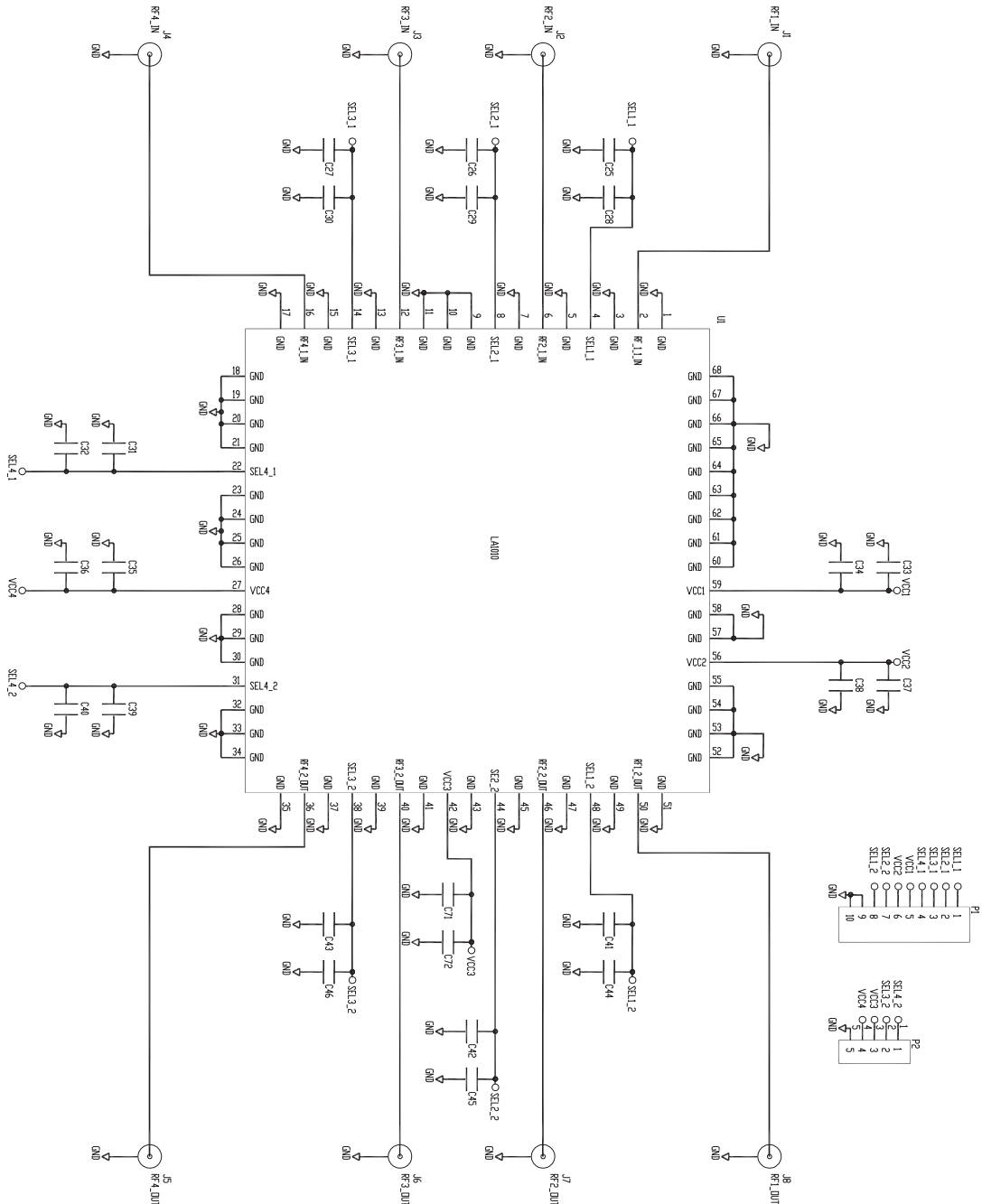
**Legend:**

- A =  $0.250 \times 0.425$  mm
- B =  $0.425 \times 0.250$  mm
- C =  $8.225 \times 8.250$  mm

[illegible]

## Evaluation Board Schematic

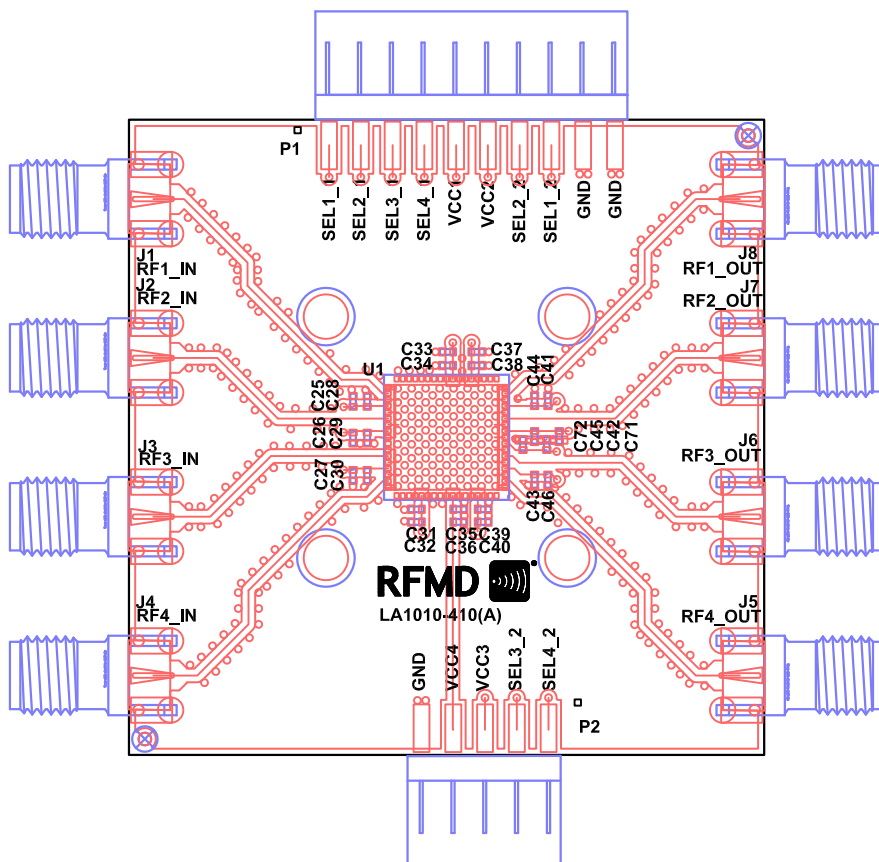
### 1920MHz to 1980MHz Application Circuit



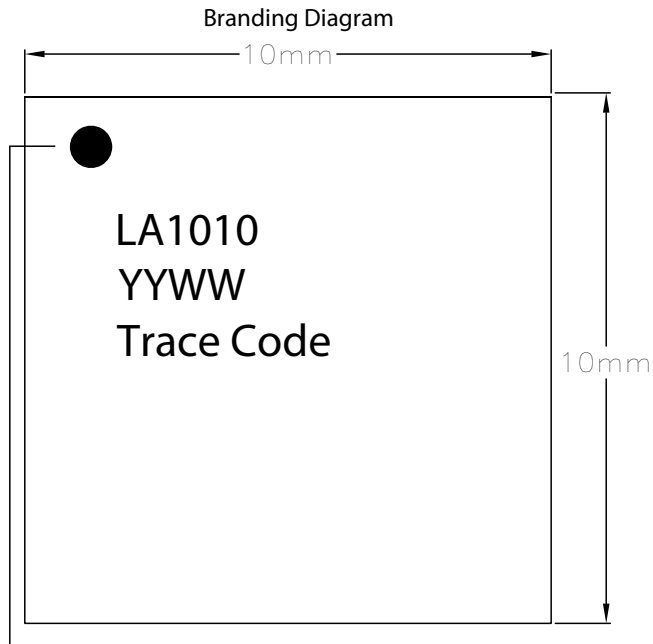
## Evaluation Board Build of Materials (BOM)

Description	Reference Designator	Manufacturer	Manufacturer's P/N
Evaluation Board		DDI	LA1018410(A)
CAP, 0.1μF, 10%, 16V, X7R, 0402	C25-C27, C32-C33, C36-C37, C40, C44-C46, C72	Murata Electronics	GRM155R71C104KA88D
CONN, SMA, END LNCH, UNIV, HYB MNT, FLT	J1-J8	HEILIND ELECTRONICS	PER MAT-21-1038
CONN, HDR, ST, PLRZD, 10-PIN	P1	ITW Pancon	MPSS100-10-C
CONN, HDR, ST, PLRZD, 5-PIN, 0.100"	P2	ITW Pancon	MPSS100-5-C
DNI	C28-C31, C34-C35, C38-C39, C41-C43, C71		
Two stage LNA plus SAW	U1		RFLA1010SB

## Evaluation Board Assembly Drawing



## Evaluation Board Assembly Drawing



Fill in the YYWW Notation with the Date Code

YY = Year

WW = Week

Trace Code to be assigned by SubCon