

VFVX301

VCXO Low Jitter 2.5V, 3.3V

5x7mm SMD, LVPECL / LVDS



Features

- 38MHz to 800MHz frequency range
- Ultra low phase noise
- <0.5 ps RMS jitter over 12kHz - 20MHz
- APR to ± 150 ppm



RoHS Status



Applications

- Optical Networking, SONET / SDH
- 10 Gigabit Ethernet
- Broadband Access

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Frequency Range	F		38 38		800 640	MHz	3.3V 2.5V
Frequency Stability	$\Delta F/F$	Vs. Operating Temperature			± 50 ± 25 ± 20	ppm	Order Code B Order Code C Order Code D
		Vs. Supply Voltage		± 1.5	± 3	ppm/V	
		Vs. Aging / Year		± 3 ± 1		ppm ppm/y	First Year After first year
Operating Temperature	T		0° -40°		+70° +85°	°C	Order Code B Order Code G
Output		LVPECL LVDS	Available up to 800MHz Available up to 640MHz				Order Code L Order Code D
Supply Voltage	V _{CC}		3.15 2.375	3.3 2.5	3.45 2.625	V	Order Code E Order Code G
Voltage Control	V _C		0 0		3.3 2.5	V	0.3 – 3.0 available
APR			100	150		ppm	
Period RMS Jitter		77.76MHz 155.52MHz 311.08MHz 622.08MHz		2.5 3 3 6	4 4 5 8	ps	
Integrated RMS Jitter 12kHz to 20MHz		155.52MHz 311.04MHz 622.08MHz		0.4 0.4 0.4	0.5 0.5 0.5	ps	
Period Jitter Peak-to-Peak		77.76MHz 155.52MHz 311.08MHz 622.08MHz		18 20 25 42	30 30 30 55	ps	
VCON Modulation Bandwidth	BW	0V < VCON < 3.3V	25			kHz	



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Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Symmetry		($V_{DD}-1.3$) V_{DC} 1.25 V_{DC}	45 45		55 55	%	PECL LVDS
Phase Noise		10Hz 100Hz 1kHz 10kHz 100kHz 1MHz		-66 -96 -124 -136 -132 -145		dBc/Hz	@77.76MHz
		10Hz 100Hz 1kHz 10kHz 100kHz 1MHz		-62 -92 -120 -132 -128 -144		dBc/Hz	@155.52MHz
		10Hz 100Hz 1kHz 10kHz 100kHz 1MHz		-59 -86 -116 -129 -124 -140		dBc/Hz	@311.04MHz
		10Hz 100Hz 1kHz 10kHz 100kHz 1MHz		-48 -80 -108 -118 -114 -131		dBc/Hz	@622.08MHz
Supply Current	I_{CC}	38 – 100MHz 100 – 300MHz 300 – 800MHz			65 80 90	mA	PECL
		38 – 100MHz 100 – 320MHz 320 – 640MHz			45 60 70	mA	LVDS
Load	50 Ohms to $V_{DD}-2V$ (PECL) 100 Ohms (LVDS)						
Output High Voltage	V_{OH}		$V_{DD}-1.025$ 1.4		1.6	V	PECL LVDS
Output Low Voltage	V_{OL}		0.9	1.1	$V_{DD}-1.620$	V	PECL LVDS
Output Differential Voltage	V_{OD}		247	355	454	mV	LVDS
Offset Voltage	V_{OS}		1.125	1.2	1.375	V	LVDS
Rise / Fall Time	T_R/T_F	20% to 80%		0.6 0.7	1.5 1.0	ns	PECL LVDS
Tristate	"1": Output Enable – Pin 2 may float or 2.8V min (3.3V V_{DD}) or 2.25V min (2.5V V_{DD}) "0": Tristate – Pin 2 requires 0.4V max (3.3V or 2.5V V_{DD})						

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Lead Temperature		Soldering, 10s max			260	°C	
Storage Temperature	T _S		-55		+125°	°C	
Junction Temperature	T _J				+125°	°C	
Supply Voltage	V _C		-1		4.6	V	
ESD Protection		Human Body Model			2	kV	

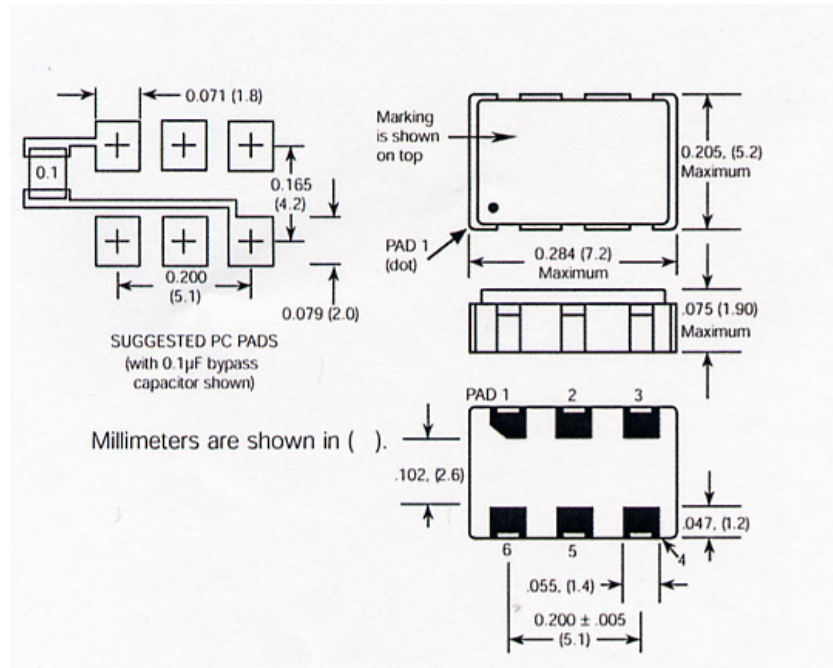
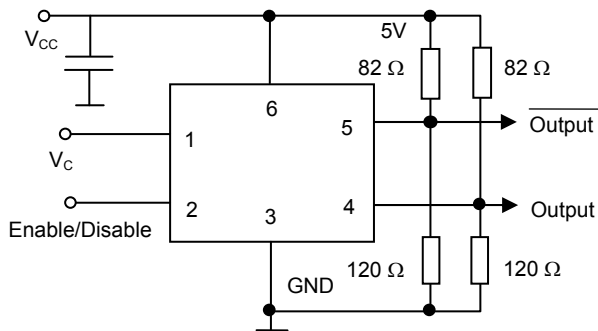
Environmental and Mechanical Conditions

Parameter	Conditions
Shock	1000 Gs, 0.35ms, ½ sine wave, 3 shocks in each plane
Humidity	Resistant to 85 °R.H. at 85 °C
Vibration	10-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less
Leak	Leak rate less than 5x10 ⁻⁸ atm.cc/s of helium (crystal only)
Case	Ceramic with hermetic resistance-welded metal lid
Pads	Solderable gold over nickel
Marking	Epoxy ink or laser engraved
Resistance to Solvents	MIL STD 202, Method 215

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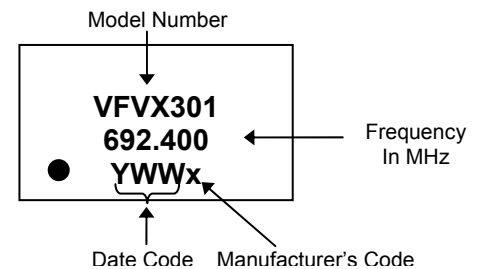
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Pin Assignments

Pin #	Connection
1	V _C
2	Tristate
3	Case, GND
4	Output
5	Output
6	Supply Voltage

Marking Specification



How to Order

