QPB9011

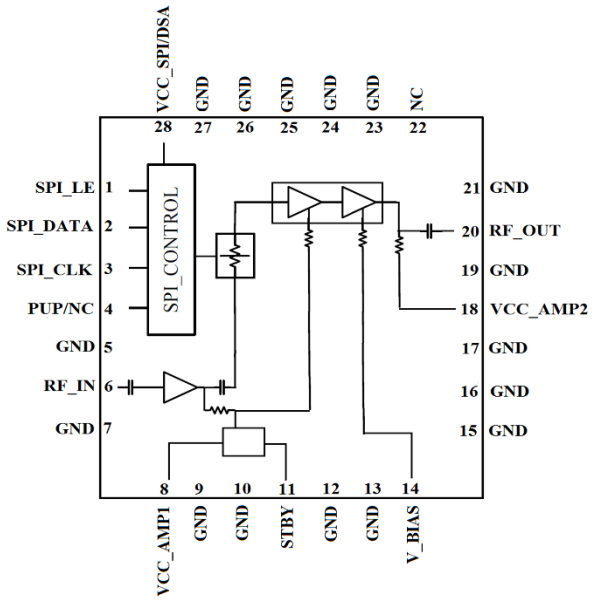
2.3-2.7 GHz 2 W Digital Variable Gain Amplifier

Product Overview

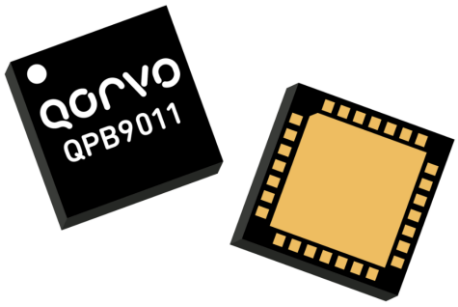
The QPB9011 is a digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. This amplifier module integrates gain blocks, a digital-step attenuator (DSA), and a high linearity 2 W amplifier. The module has the added feature of integrating all matching components, bias chokes and blocking capacitors. The internal 6-bit DSA provides a 31.5 dB gain control range in 0.5 dB steps, controlled with a serial periphery interface (SPI™). The module is integrated with low current amplifier shutdown capability.

The QPB9011 features variable gain from 12.5 dB to 44 dB at 2.6 GHz, +37 dBm output IP3 (at ATTN = 10dB), and +32 dBm P1dB. The module operates from a single +5V supply and is available in a compact 28-pad 6x6 mm leadless SMT package.

Functional Block Diagram



Top View



28 Pad 6 x 6 x 0.91 mm Package

Key Features

- 2.3-2.7 GHz Frequency Range
- 44 dB Maximum Gain at 2.6 GHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +37 dBm Output IP3 (at ATTN = 10dB)
- +32 dBm Output P1dB
- ACLR -50dBc, LTE 20MHz, Pout 20dBm
- Fully Internally Matched Module
- Integrated Blocking Capacitors, Bias Inductors
- Integrated Amplifier Shutdown Function
- 3-wire SPI Control

Applications

- Wireless Infrastructure
- CDMA, WCDMA, LTE
- TDD or FDD Systems

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150°C
RF Input Power, 50Ω, T = 25°C	+TBD dBm
V_{DD}, Power Supply Voltage	+5.5 V
Digital Input Voltage	V_{CC}+0.5V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC} (pins 8, 14, 18)	+4.75	+5.0	+5.25	V
Case Temperature	−40		+105	°C
Tj (for>10^6 hours MTTF)			170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions [1]	Min	Typ	Max	Units
Operational Frequency		2300		2700	MHz
Test Frequency			2600		MHz
Gain			44		dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Attenuation Accuracy	3 wire SPI, 6 states	± (0.3 + 4% of Atten. Setting) Max			dB
Attenuation Step			0.5		dB
Step Error			+/-0.3		dB
Control Interface	3-wire SPI		6		Bit
Input Return Loss			10		dB
Output Return Loss			7		dB
Output P1dB			32		dBm
Output IP3	Pout =+17 dBm/tone, Δf=1MHz, ATTN = 10dB		37		dBm
ACLR	Pout=+20dBm, LTE 20MHz, ATTN = 10dB		-50		dBc
Noise Figure			4.3		dB
I/O Impedance			50		Ω
Supply Voltage	VCC_AMP1, VCC_AMP2, VCC_SPI/DSA, V_BIAS		+5		V
Supply Current, I_{CC}	Powered Down		2		mA
	Powered Up, Quiescent		225		mA
	Powered Up, Pout at 17dBm		300		mA
Control Voltage, V_{STBY}	Powered Down	-0.2		0.63	V
	Powered Up	1.17		3.3	V
Control Current, I_{STBY}	Powered Down or Powered Up		200		uA
Settling Time	T_{ON}, T_{OFF} (50% control to 10% / 90% RF)		TBD		µS
Thermal Resistance, θ_{jc}	Module (junction to case)			TBD	°C/W

1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, Temp = +25 °C, 50 Ω system.

Serial Control Interface

The QPB9011 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DSA to the minimum gain state. The 6-bit SID (Serial Input Data) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled.

Serial Control Timing Characteristics (Test conditions: V_{CC} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
t1	CLK Frequency		25	MHz
t2	CLK High	20		Ns
t3	CLK Low	20		ns
t4	SERIN to CLK Setup Time	5		ns
t5	SERIN to CLK Hold Time	5		ns
t6	SERIN Valid	30		
t7	LE to CLK Setup Time	5		
t8	CLK to LE Setup Time	5		ns
t9	LE Pulse Width	10		ns

Serial Control DC Logic Characteristics (Test conditions: V_{CC} = +5 V, Temp.=25°C)

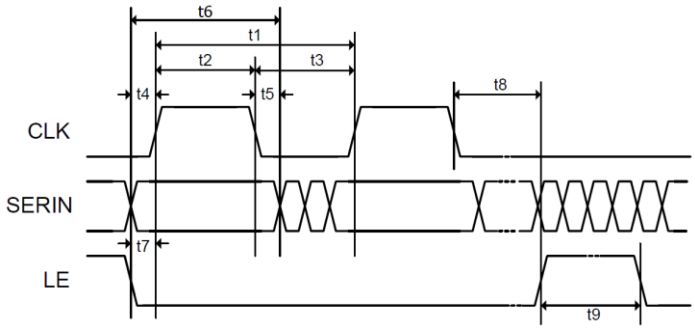
Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		-0.2	0.63	V
Input High State Voltage, V_{IH}		1.17	V_{CC_SPI}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−0.95	+0.95	µA
Power up reset time, T_{rs}			500	µS
V_{CC_SPI} Supply ramp time, T_r		10		µS
Input Current, I_{CC_SPI}			180	uA

SERIN Control Logic Truth Table

6-Bit Control Word						Attenuation State
MSB					LSB	
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference: IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

Any combination of the possible 64 states will provide an attenuation of the sum of bits selected.

Timing Diagram



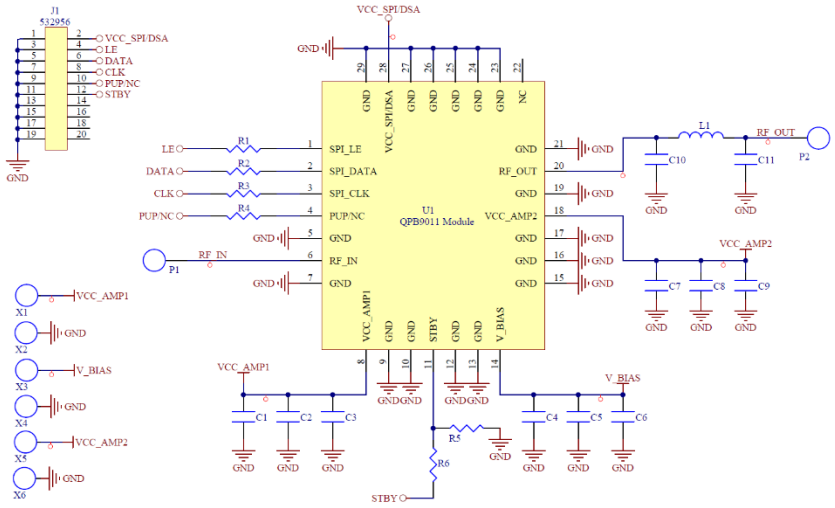
STBY Control Logic Truth Table

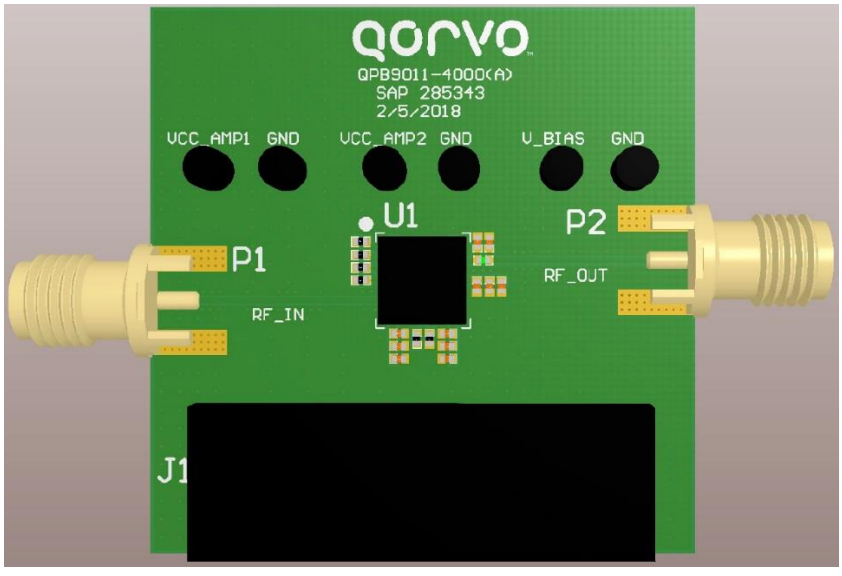
Pin	State	Amplifiers Operation
11, STBY	Low	Powered Down
	High	Powered Up

Power-up State Logic Truth Table

Pin	State	Attenuation Setting
4, PUP	Low	Relative Attenuation at Minimum, 0dB
	High	Relative Attenuation at Maximum, 31.5dB

QPB9011 – Evaluation Board





Bill of Material – QPB9011EVBP02

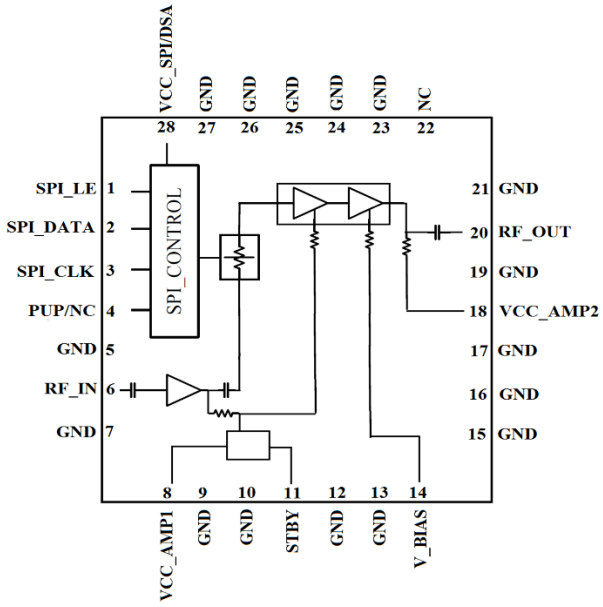
Reference Des.	Value	Description	Manuf.	Part Number
PCB		Printed Circuit Board	Qorvo	
U1		DVGA, QPB9011, 2.3-2.7GHz	Qorvo	QPB9011
L1	100pF	Cap, 100pF, 5%, 50V, C0G, 0402	various	
R1, R2, R3, R4, R6	0 Ω	Res, 0 Ω, Jumper, 0402	various	
P1, P2		Conn, SMA End Launch, 0.07 pin	various	
J1		Conn, Receptacle, 20pos., 100RT/A, Dual	various	
X1, X2, X3, X4, X5, X6		Term. Solder Turret, .062 PCB	various	

QPB9011EVBP02 Typical Performance

Parameter	Conditions	Typical Value					Units
Frequency		2300	2400	2500	2600	2700	MHz
Gain		44.7	46.9	45.6	44.3	43.0	dB
Input Return Loss		15.6	14.7	12.6	11.7	11.6	dB
Output Return Loss		6.5	6.4	7.0	8.0	8.7	dB
Output P1dB		31.6	31.7	31.8	-	32.1	dBm
Output IP3	Pout=17 dBm/tone, Δf= 1 MHz, ATTN 10dB	38.8	38.8	38.2	37.6	36.9	dBm
ACPR	Pout=20dBm, ATTN 10dB, LTE 20MHz	-56.7	-56.7	-53.6	-	-48.3	dBc
Noise Figure		4.13	4.15	4.20	4.23	4.3	dB
Vcc Supply Current, I_{CC} Total	Pout=17dBm	270	-	-	-	300	mA

Notes:
1. Test Conditions: V_{CC} = +5V, Temp.=+25 °C

Pad Configuration and Description

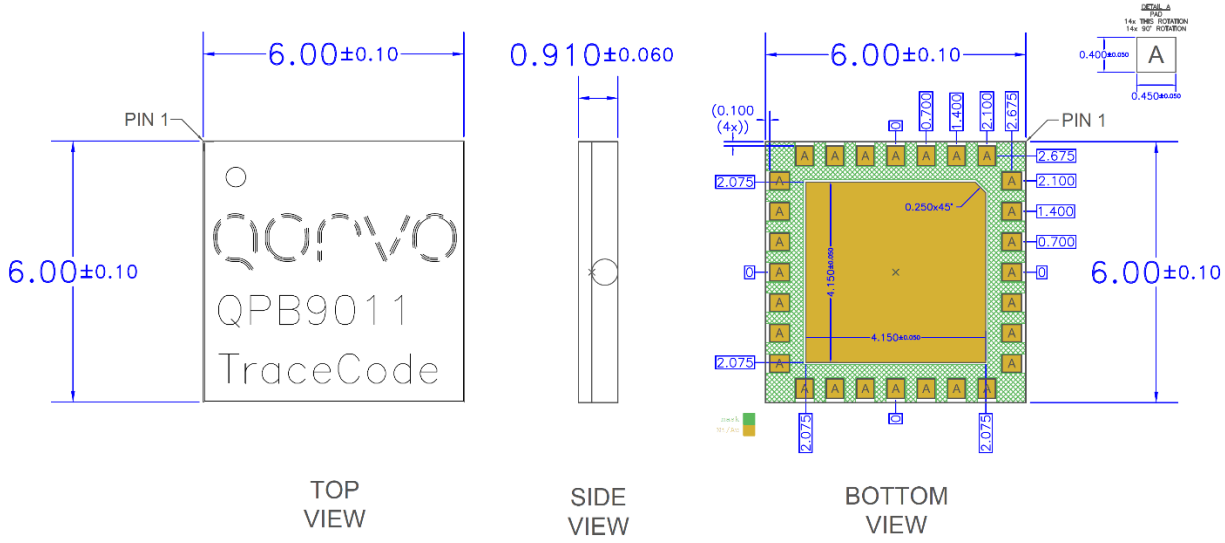


Top View

Pad No.	Label	Description
1	SPI_LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	SPI_DATA	Serial data input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	SPI_CLK	Serial clock input.
4	PUP/NC	Power up programming pin; NC for “do not care”
6	RF_IN	Input, matched to 50 ohms. Internally DC blocked.
8	VCC_AMP1	Supply Voltage to AMP1.
11	STBY	Standby. With Logic Low the amplifier is powered off with the SPI still powered on.
14	V_BIAS	Additional Supply Voltage
18	VCC_AMP2	Supply Voltage for AMP2/AMP3.
20	RF_OUT	Output matched to 50 ohms. Internally DC blocked.
22	NC	Do not connect, leave open circuit
28	VCC_SPI/DSA	SPI and DSA DC supply.
5, 7, 9, 10, 12, 13, 15-17, 19, 21, 23-27	GND	RF/DC Ground Connection
Backside Paddle	GND	RF/DC Ground Connection

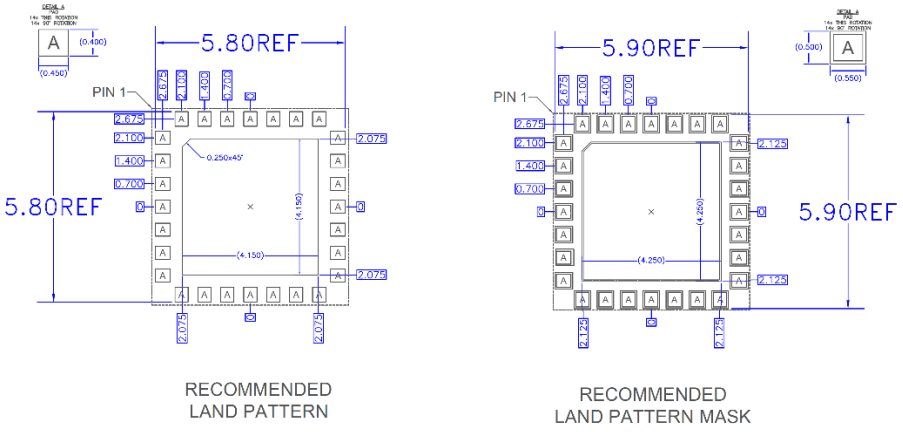
Package Marking and Dimensions

Marking: Pin 1 Dot and Qorvo Logo
Part Number – QPB9011
Trace Code – XXXXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: NiPdAu

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class TBD	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class TBD	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment). This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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