Part Number: IGT5259M25 preliminary

Integra
TECHNOLOGIES, INC.

C-Band Radar 50Ω Transistor

Part number IGT5259M25 is a high power transistor which is internally matched to 50 ohms. It is designed for C-Band radar applications and operates over the instantaneous bandwidth of 5.2 – 5.9 GHz. It utilizes gold metal gallium nitride (GaN) high electron mobility transistor (HEMT) technology operating in common source configuration. Under 300us / 10% pulse conditions it supplies a minimum of 25 watts of peak output power with 13dB gain typically. Specified operation is with Class AB bias. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of P_{PEAK} = 25W @ 10% duty factor. This corresponds to an average power P_{AVG} = 2.5W.

50 Ohm Matched
- Requires no external impedance matching circuitry

GaN on Silicon Carbide FET
- High Power Gain
- Excellent thermal stability
- Gold Metal

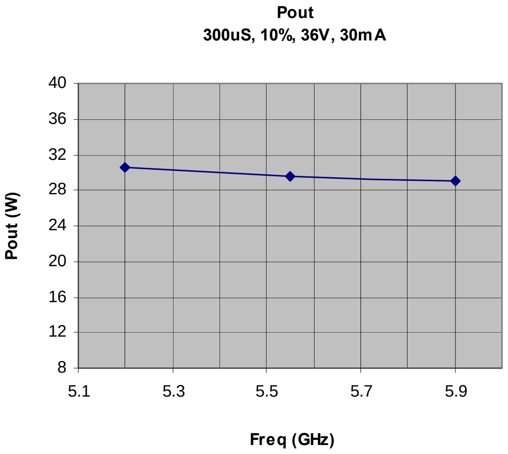
Depletion Mode Device
- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

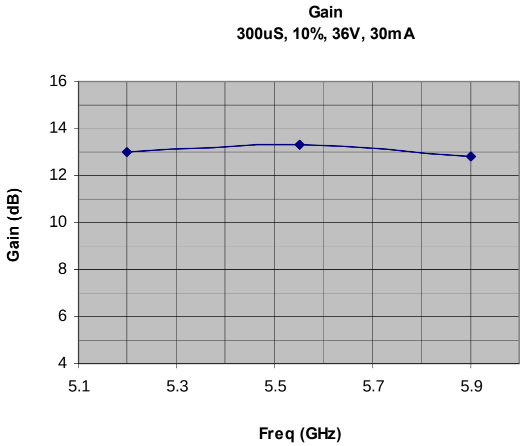
Gold Metal System
- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

BeO Free Package
- Metal Based
- Epoxy Seal

High Power RF Test / Fixture
- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed

DEVELOPMENT RF DATA





MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Breakdown Voltage	$V_{DS\text{-}BK}$	--	80	V	--
BD	Drain-Source Voltage	V_{DS}	--	40	V	--
BD	Gate-Source Voltage	V_{GS}	-10	0	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.40	°C/W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25±5°C, P_{OUT}=25W
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

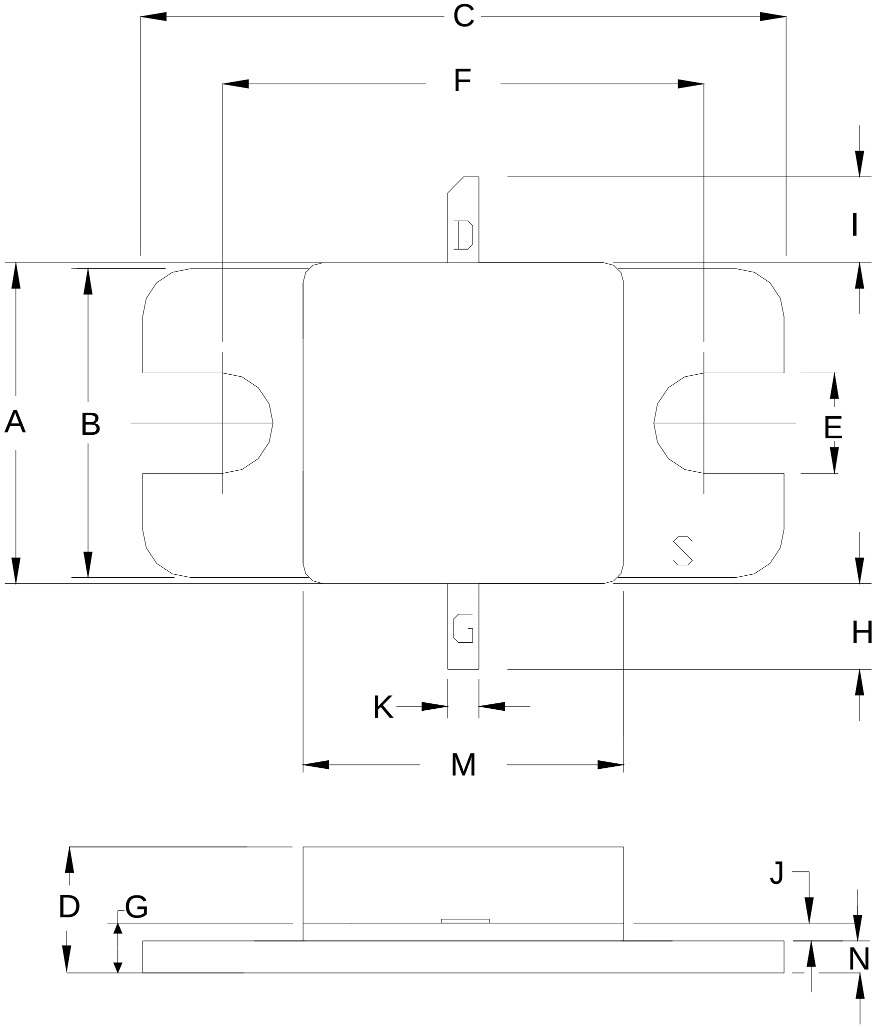
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage Current	$I_{D\text{-}OFF}$	--	0.3*	--	mA	V_{GS}= -8V, V_{DS}= 36V, T_F = 25±5°C, *Typical Only.
100%	Gate Threshold Voltage	$V_{GS\text{-}TH}$	--	-3.5*	--	V	V_{DS}= 36V, I_D= 30mA, T_F = 25±5°C, *Typical Only.

RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-20	-10	-7	dB	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ PW=PW1, DF=DF1, T_F=$T_{F1,}$ P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5.
100%	Power Gain	Gp	12.0	13.0	14.0	dB	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ PW=PW1, DF=DF1, T_F=$T_{F1,}$ P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5
100%	Drain Efficiency	N_D	45	50	75	%	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ PW=PW1, DF=DF1, T_F=$T_{F1,}$ P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5
100%	Pulse Amplitude Droop	D	-0.50	-0.10	0.30	dB	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ PW=PW1, DF=DF1, T_F=$T_{F1,}$ P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5
100%	Delta Insertion Phase	DIP	-30	--	+30	DEG	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ PW=PW1, DF=DF1, T_F=$T_{F1,}$ P_{IN}=P_{IN1}, F=F5.
100%	3:1 Load Mismatch Stability	VSWR-S	3:1		--	--	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ PW=PW1, DF=DF1, T_F=$T_{F1,}$ P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5 Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least –65 dBc.
Note 1	V1 = 36V; I_{DQ1} = 30mA; PW1 = 300us; DF1 = 10%, P_{IN1} = 1.58W, P_{OUT1} = 25W.						
Note 2	Test Frequencies: F1 = 5.20 GHz, F2 = 5.55 GHz, F3 = 5.9 GHz						
Note 3	T_{F1} = 30±5°C = Device flange temperature.						
Note 4	Screen 'BD' = parameter qualified By Design.						

PACKAGE DIMENSIONAL OUTLINE DRAWING

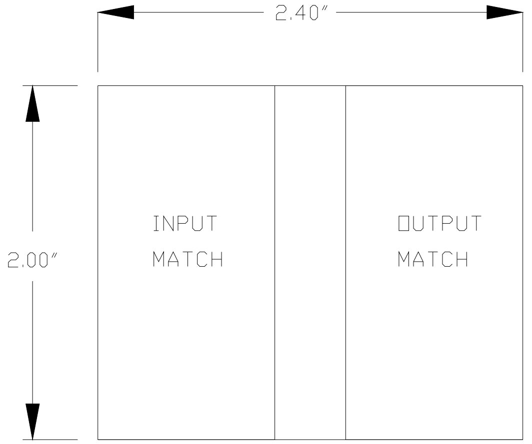


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.395	0.405	10.03	10.29
B	0.380	0.390	9.65	9.91
C	0.795	0.805	20.19	20.45
D	0.143	0.167	3.63	4.24
E	0.120	0.130	3.05	3.30
F	0.595	0.605	15.11	15.37
G	0.053	0.067	1.35	1.70
H	0.092	0.122	2.34	3.10
I	0.092	0.122	2.34	3.10
J	0.018	0.022	4.57	5.56
K	0.034	0.044	0.86	1.12
M	0.393	0.405	9.98	10.29
N	0.035	0.045	0.89	1.14

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

LID-PL44-1

RF TEST FIXTURE



CONTACT FACTORY FOR DETAILED RF TEST FIXTURE CAD DRAWING

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

DISCLAIMER