TGF3020-SM

4 – 6 GHz, 32 V, 5 W GaN RF Input-Matched Transistor

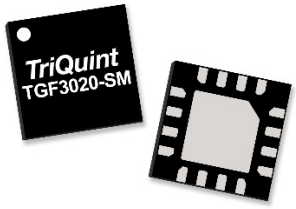
Product Overview

The Qorvo TGF3020-SM is a 5W (P_{3dB}), 50Ω-input matched discrete GaN on SiC HEMT which operates from 4.0 to 6.0 GHz. The integrated input matching network enables wideband gain and power performance, while the output can be matched on board to optimize power and efficiency for any region within the band.

The device is housed in an industry-standard 3 x 3 mm surface mount QFN package.

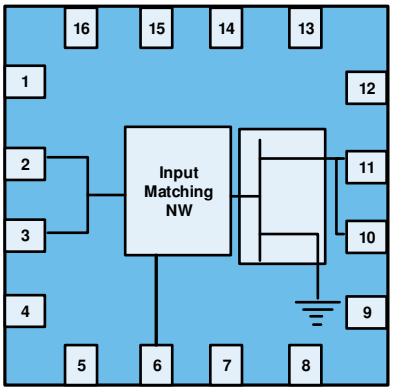
Lead-free and ROHS compliant

Evaluation boards are available upon request.



3 x 3mm QFN package

Functional Block Diagram



Key Features

- Frequency: 4 to 6 GHz
- Output Power (P_{3dB})[1]: 6.8 W
- Linear Gain[1]: 13 dB
- Typical PAE_{3dB}[1]: 60%
- Operating Voltage: 32 V
- CW and Pulse capable

Note 1: @ 5 GHz Load Pull

Applications

- Telemetry
- C-band radar
- Communications
- Test instrumentation
- Wideband amplifiers
- 5.8GHz ISM

Ordering info

Part No.	ECCN	Description
TGF3020-SM	EAR99	QFN Packaged Part
TGF3020-SMEVBP01	EAR99	5.3 – 5.9 GHz EVB
TGF3020-SMEVBP02	EAR99	4 – 6 GHz EVB

Absolute Maximum Ratings[1]

Parameter	Rating	Units
Breakdown Voltage,BV_{DG}	+100	V
Gate Voltage Range, V_G	-7 to +2.0	V
Drain Current, I_{DMAX}	0.6	A
Gate Current Range, I_G	See page 16.	mA
Power Dissipation, P_{DISS}[2]	7.5	W
RF Input Power, CW, T = 25 °C	+30	dBm
Channel Temperature, T_{CH}	275	°C
Mounting Temperature (30 Seconds)	320	°C
Storage Temperature	–65 to +150	°C

Notes:
1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Pulsed 100uS PW, 20% DC

Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Units
Operating Temp. Range	–40	+25	+85	°C
Drain Voltage Range, V_D	+12	+32	+40	V
Drain Bias Current, I_{DQ}		25		mA
Drain Current, I_D[4]	–	0.25	–	A
Gate Voltage, V_G[3]	–	–2.8	–	V
Channel Temperature (T_{CH})	–	–	225	°C
Power Dissipation (P_D)[2,4]	–	–	9.1	W
Power Dissipation (P_D), CW[2]	–	–	6.5	W

Notes:
1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85 °C
3. To be adjusted to desired I_{DQ}
4. Pulsed, 100uS PW, 20% DC

Measured Load Pull Performance – Power Tuned[1, 2]

Parameter	Typical Values				Units
Frequency, F	4	4.4	5	5.5	GHz
Drain Voltage, V_D	32	32	32	32	V
Drain Bias Current, I_{DQ}	25	25	25	25	mA
Output Power at 3dB compression, P_{3dB}	38.4	38.3	38.3	38.2	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	50.1	50.4	49.5	53.0	%
Gain at 3dB compression, G_{3dB}	9.6	9.7	9.7	10.3	dB

Notes:
1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Load-pull characteristic Impedance, Zo = 50 Ω.

Measured Load Pull Performance – Efficiency Tuned[1, 2]

Parameter	Typical Values				Units
Frequency, F	2.7	2.9	3.1	3.3	GHz
Drain Voltage, V_D	32	32	32	32	V
Drain Bias Current, I_{DQ}	25	25	25	25	mA
Output Power at 3dB compression, P_{3dB}	37.6	36.8	37.1	36.8	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	60.1	61.5	59.6	59	%
Gain at 3dB compression, G_{3dB}	10.3	10.3	10.1	10.7	dB

Notes:
1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Load-pull characteristic Impedance, Zo = 50 Ω.

RF Characterization 5.3 – 5.9 GHz EVB – 5.4 GHz Performance[1]

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	11.7	–	dB
Output Power at 3dB compression point, P3dB	–	5.7	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	53.1	–	%
Gain at 3dB compression point, G3dB	–	8.7	–	dB

Notes:

1. V_D = +32 V, I_{DQ} = 25 mA, Temp = +25 °C, Pulse Width = 100 uS, Duty Cycle = 20%

RF Characterization 4 – 6.0 GHz EVB – 4.7 GHz Performance[1]

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	11.8	–	dB
Output Power at 3dB compression point, P3dB	–	5.6	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	51.7	–	%
Gain at 3dB compression point, G3dB	–	8.8	–	dB

Notes:

1. V_D = +32 V, I_{DQ} = 25 mA, Temp = +25 °C, Pulse Width = 100 uS, Duty Cycle = 20%

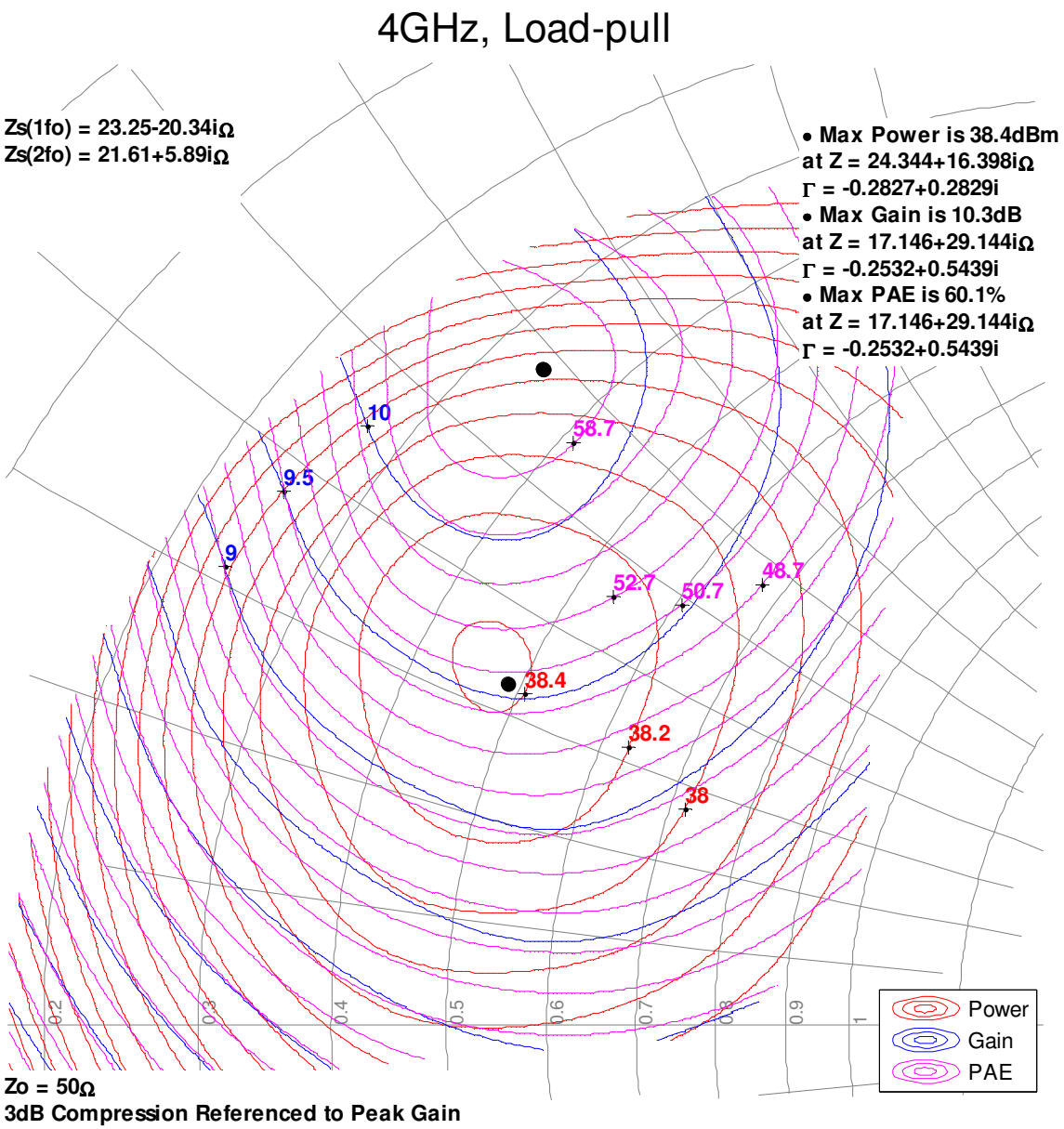
RF Characterization – Mismatch Ruggedness at 5.3 and 5.9 GHz

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 25 mA
Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector.

Measured Load-Pull Smith Charts[1, 2]

Notes:
1. Test Conditions: V_D = 32 V, I_{DQ} = 25 mA, 100 uS Pulse Width, 20% Duty Cycle
2. See page 17 for load pull reference planes where the performance was measured.



Measured Load-Pull Smith Charts[1, 2]

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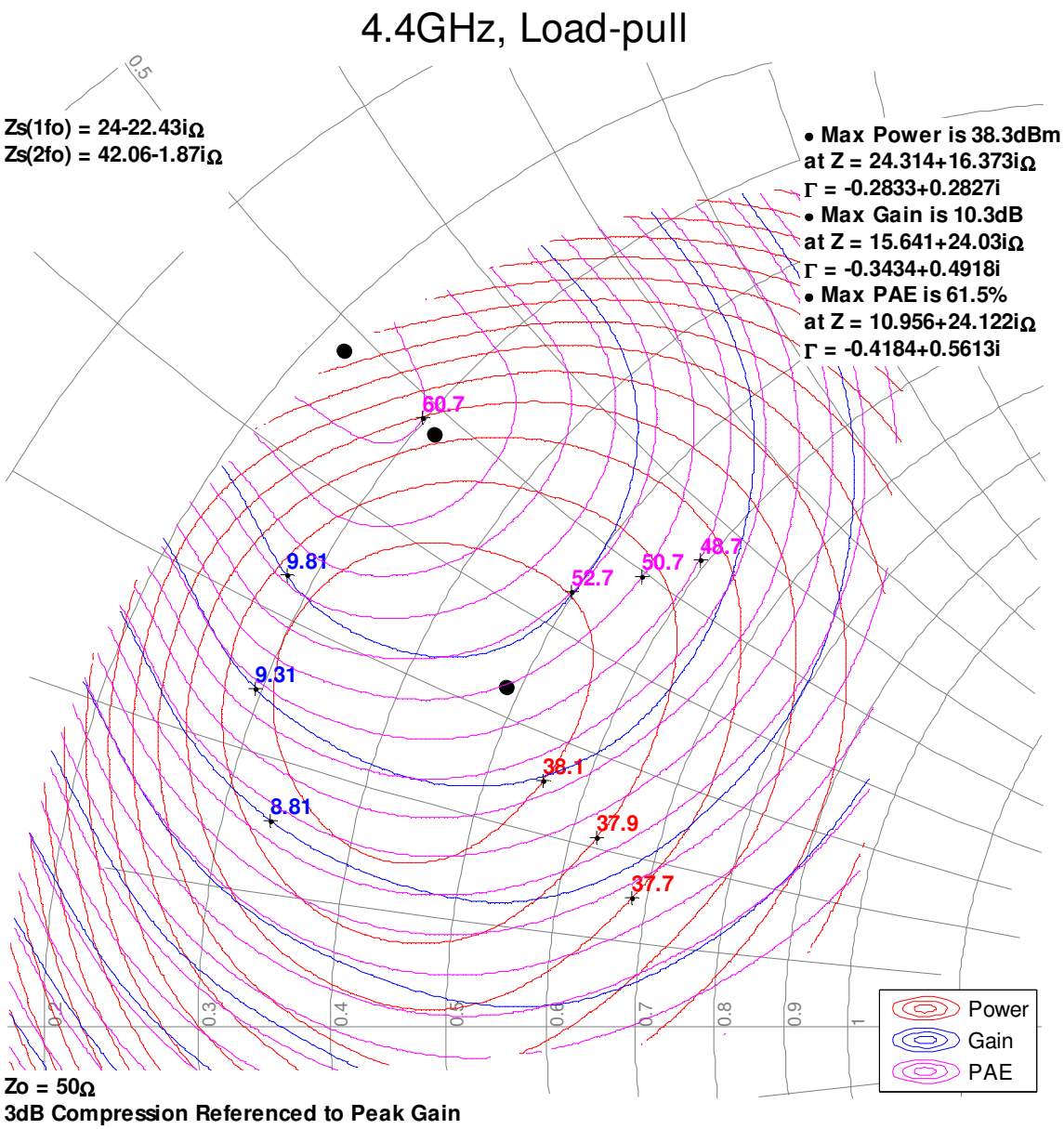

Measured Load-Pull Smith Charts[1, 2]

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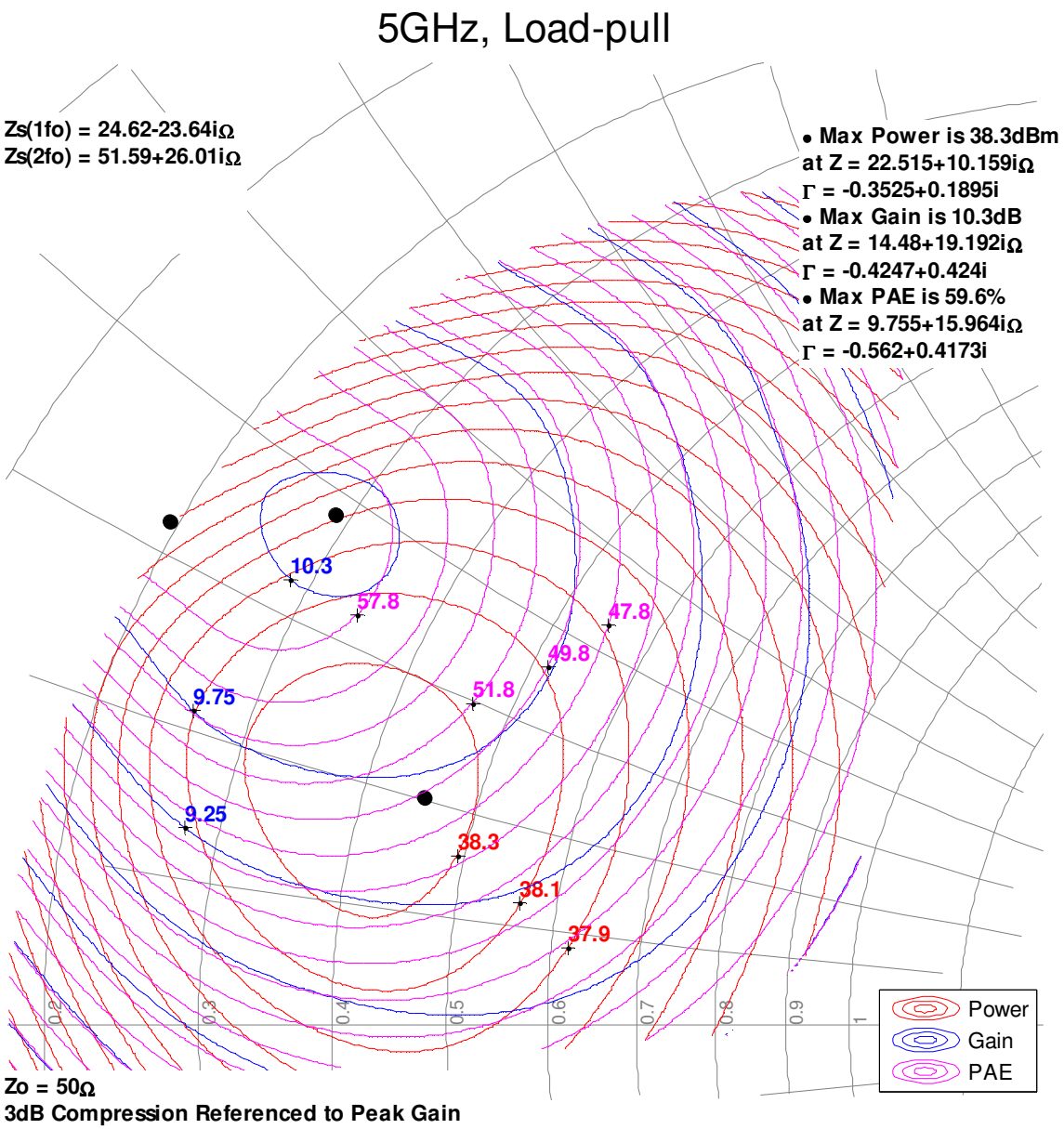

Measured Load-Pull Smith Charts[1, 2]

Notes:
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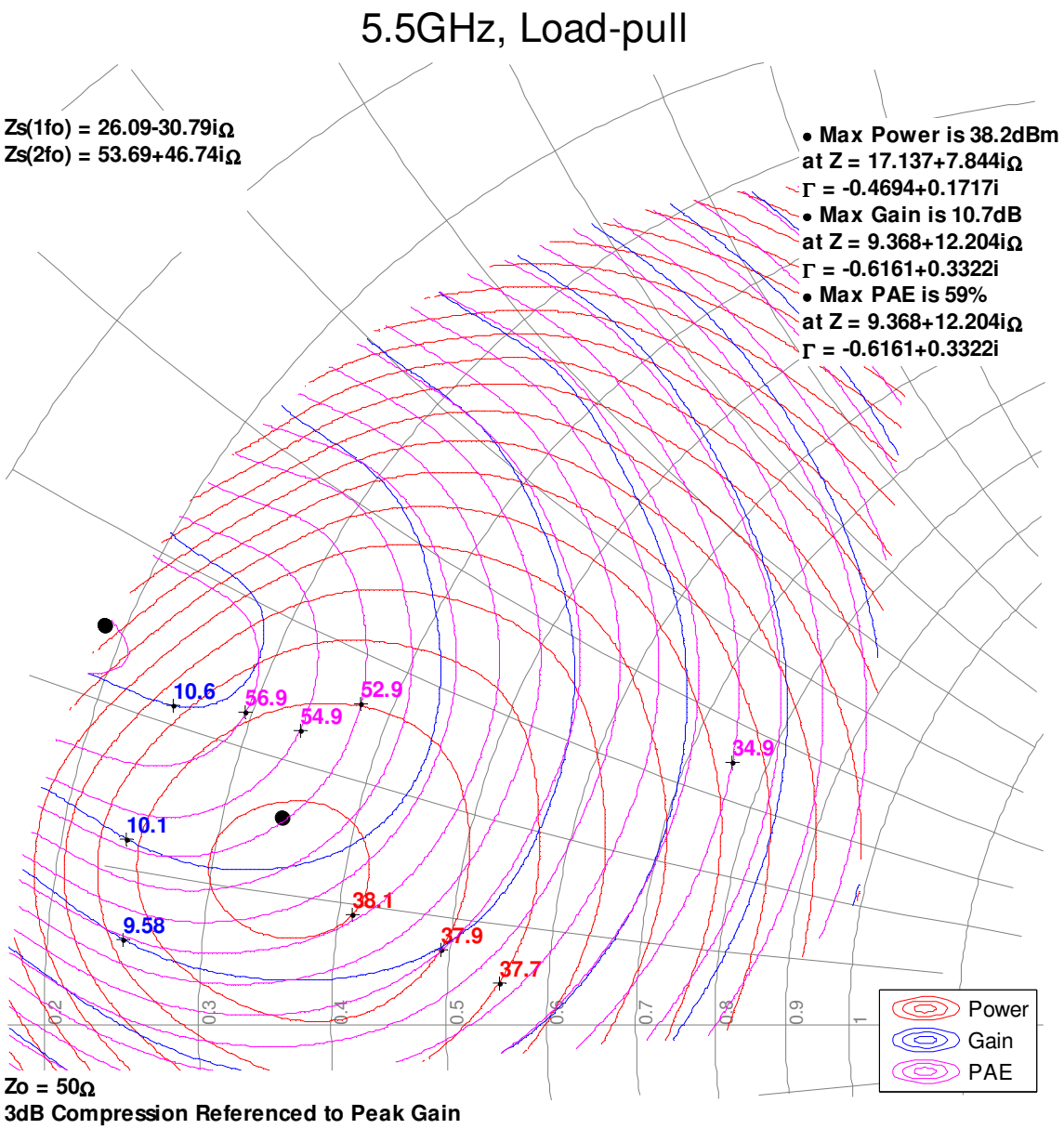
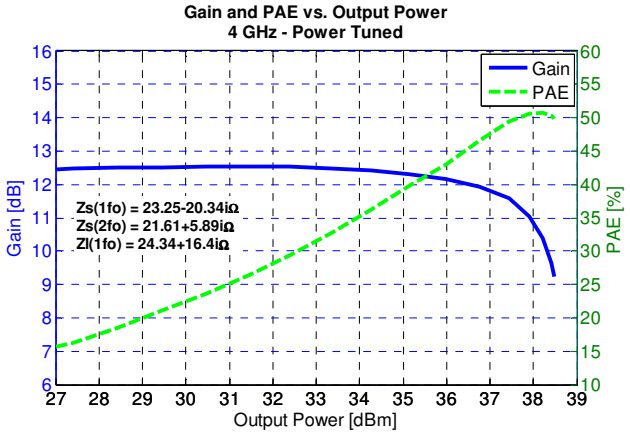
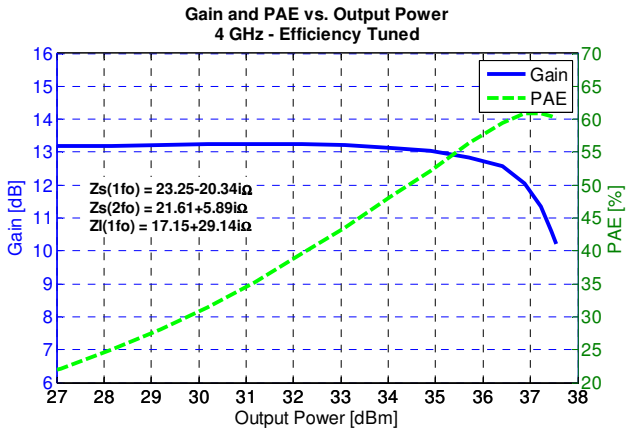
2. See page 17 for load pull reference planes where the performance was measured.

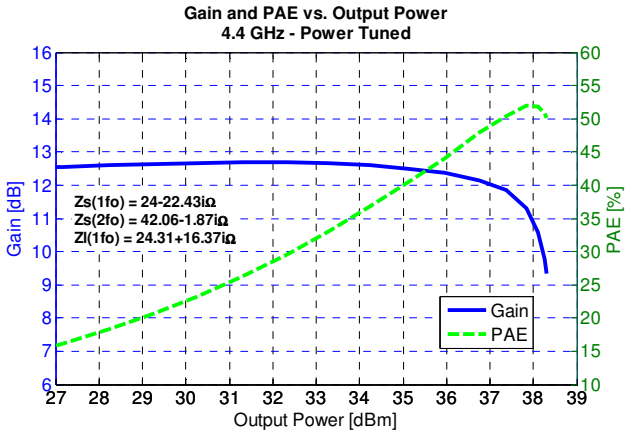


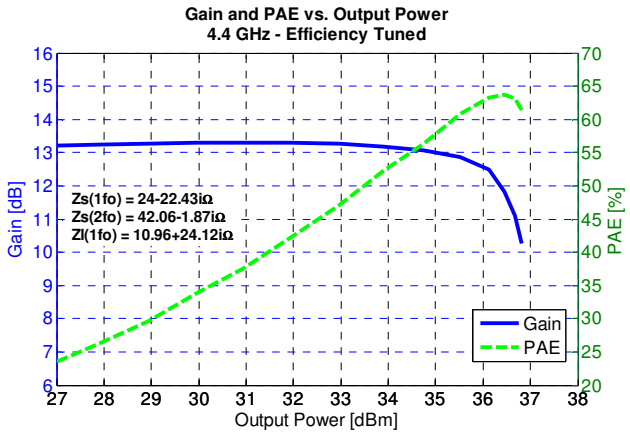
Typical Measured Performance – Load-Pull Drive-up[1, 2]

Notes:
1. Pulsed signal with 100uS pulse width and 20% duty cycle
2. See page 17 for load pull and source pull reference planes.



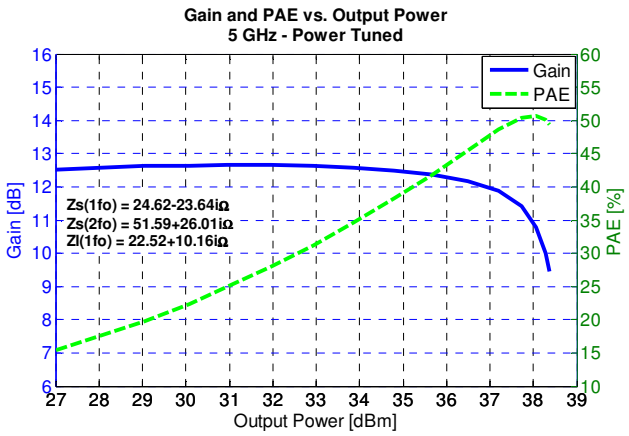


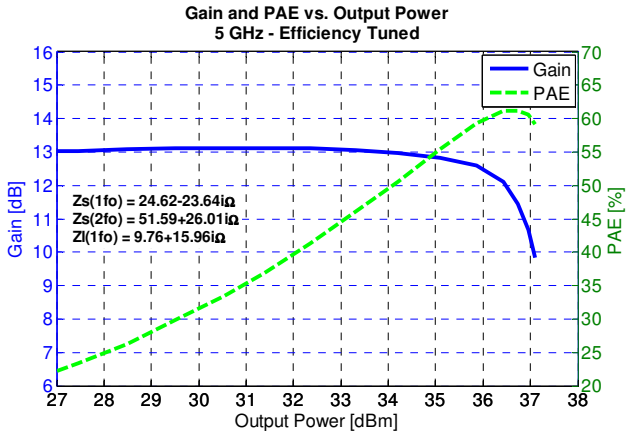


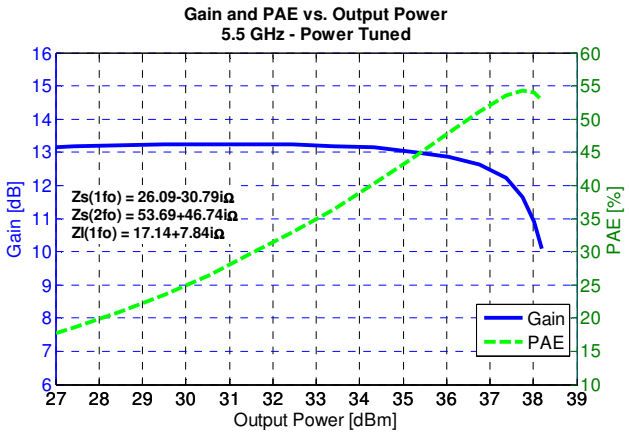


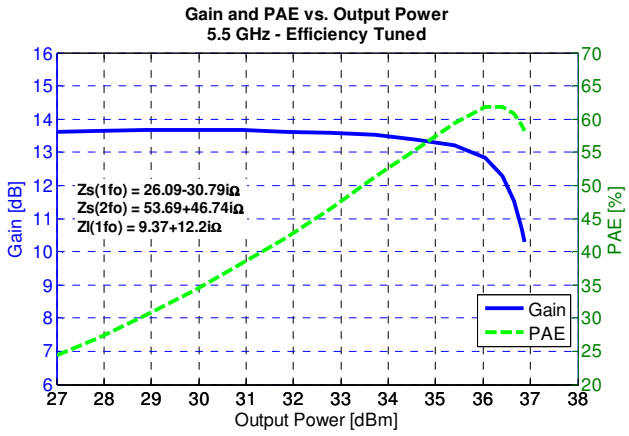
Typical Measured Performance – Load-Pull Drive-up[1, 2]

Notes:
1. Pulsed signal with 100uS pulse width and 20% duty cycle
2. See page 17 for load pull and source pull reference planes.



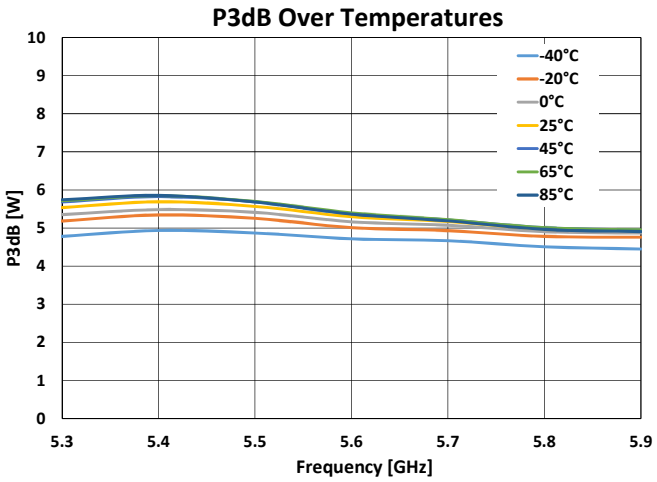


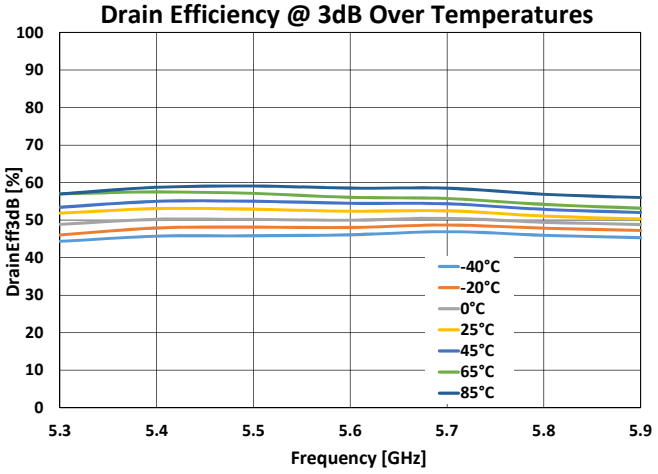


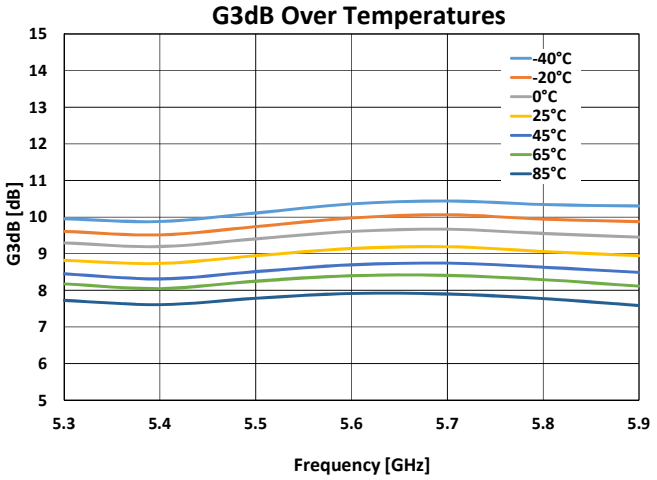


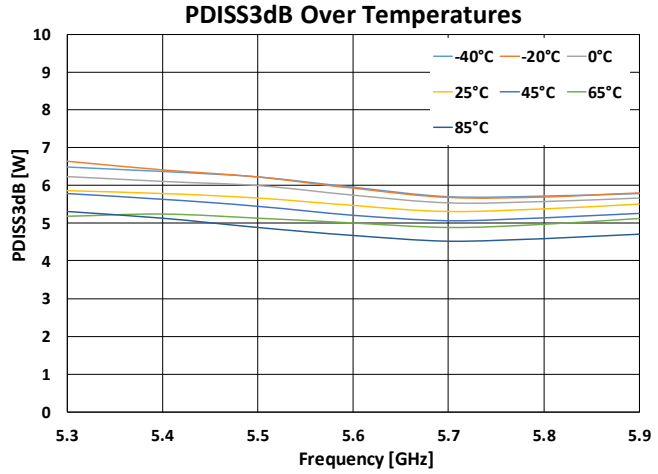
Power Driveup Performance Over Temperatures Of 5.3 – 5.9 GHz EVB[1, 2]

Notes:
1. Test Conditions: V_D = 32 V, I_{DQ} = 25 mA, 20 uS Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network.



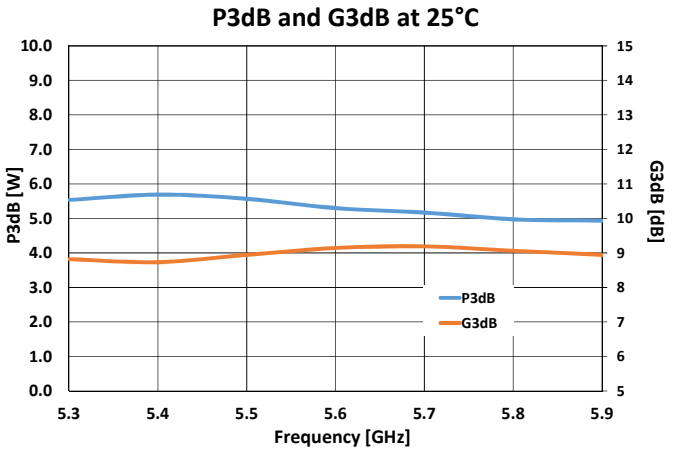


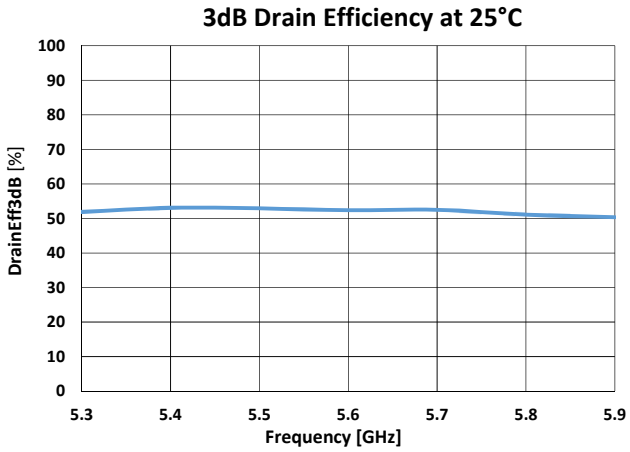


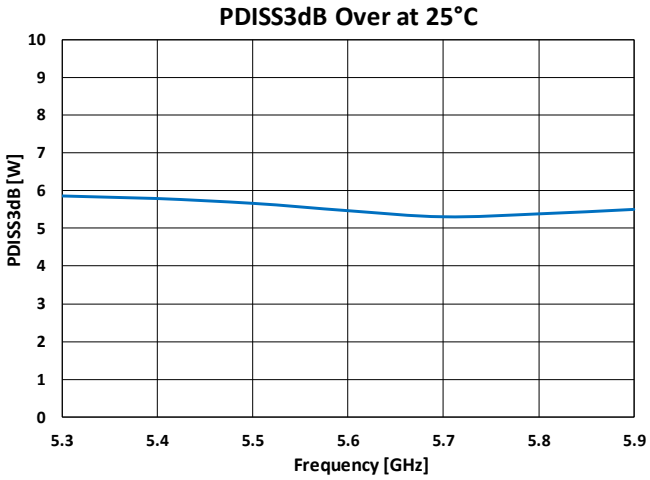


Power Driveup Performance At 25°C Of 5.3 – 5.9 GHz EVB[1, 2]

Notes:
1. Test Conditions: V_D = 32 V, I_{DQ} = 25 mA, 20 uS Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network..

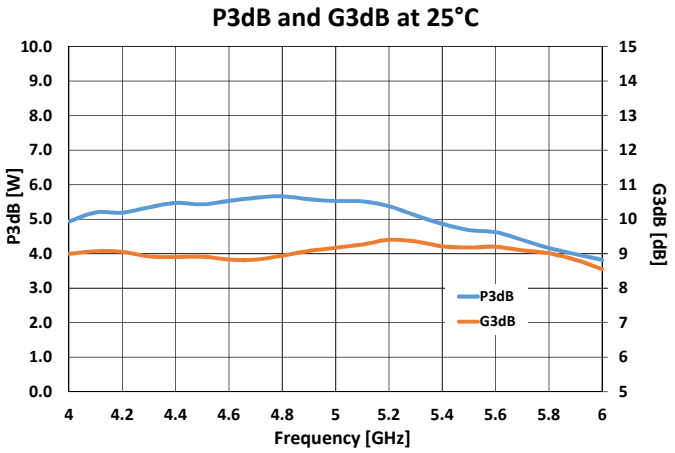


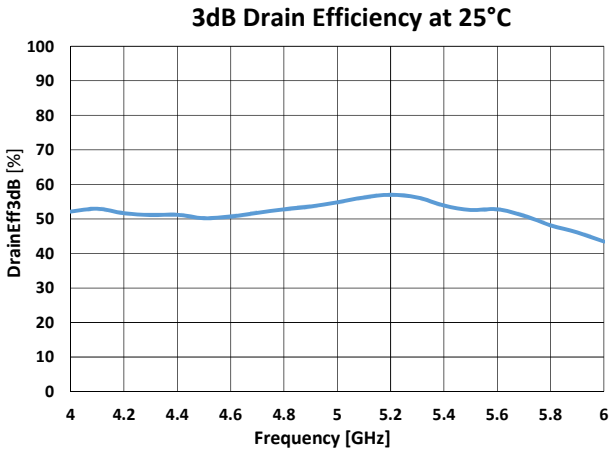


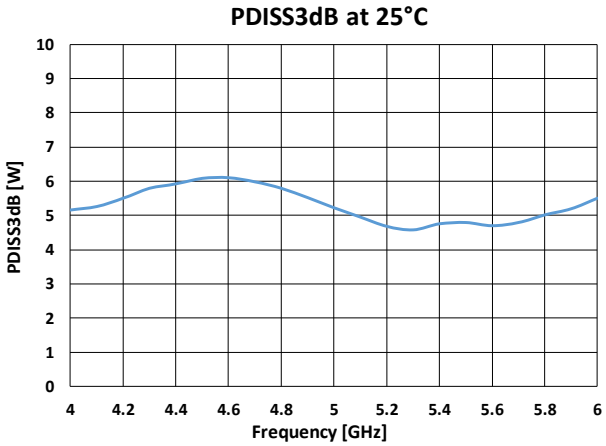


Power Driveup Performance At 25°C Of 4 – 6 GHz EVB[1, 2]

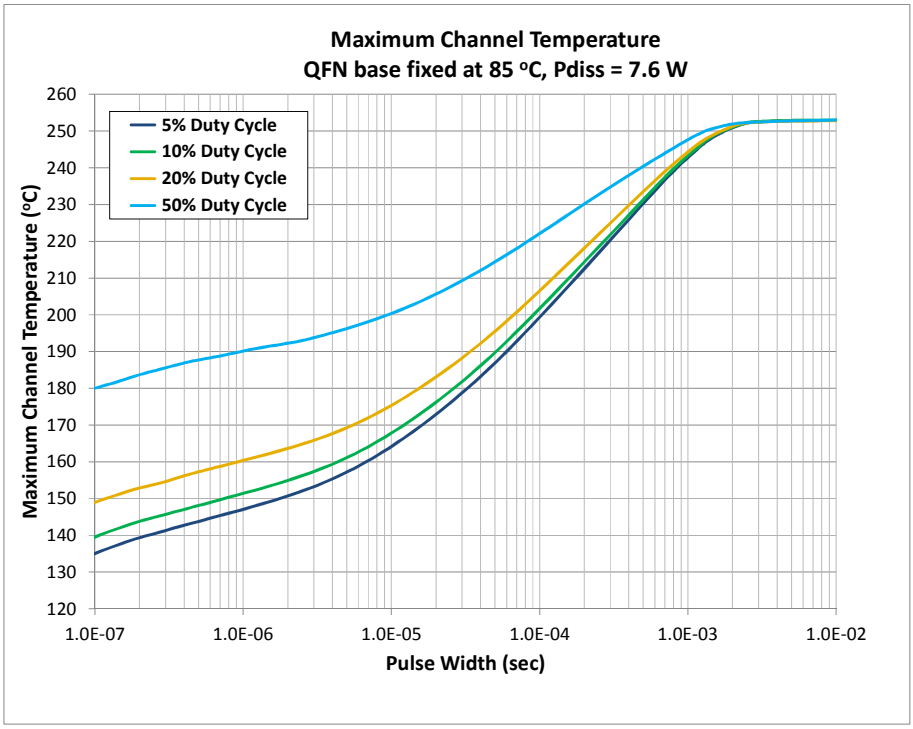
Notes:
1. Test Conditions: V_D = 32 V, I_{DQ} = 25 mA, 100 uS Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network..







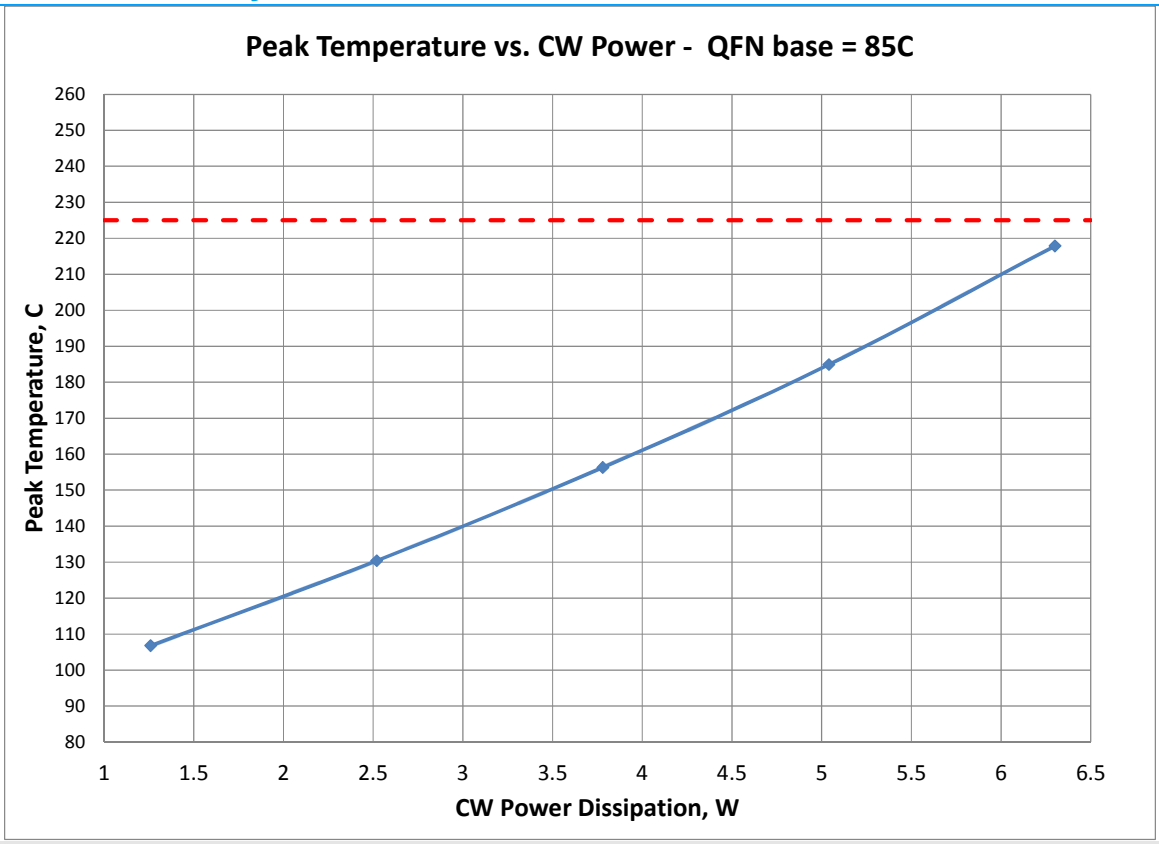
Thermal and Reliability Information – Pulsed[1, 2]



Parameter	Conditions	Values	Units
Thermal Resistance, FEA (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS PW, 5% DC	15.0	°C/W
Peak Channel Temperature, FEA (T_{CH})		199	°C
Median Lifetime, FEA (T_M)[2]		1.7E7	Hrs
Peak Channel Temperature, IR		160	°C
Thermal Resistance, FEA (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS PW, 10% DC	15.4	°C/W
Peak Channel Temperature, FEA (T_{CH})		202	°C
Median Lifetime, FEA (T_M)[2]		1.3E7	Hrs
Peak Channel Temperature, IR		162	°C
Thermal Resistance, FEA (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS PW, 20% DC	16.1	°C/W
Peak Channel Temperature, FEA (T_{CH})		207	°C
Median Lifetime, FEA (T_M)[2]		8.4E6	Hrs
Peak Channel Temperature, IR		165	°C
Thermal Resistance, FEA (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS PW, 50% DC	18.0	°C/W
Peak Channel Temperature, FEA (T_{CH})		222	°C
Median Lifetime, FEA (T_M)[2]		2.3E6	Hrs
Peak Channel Temperature, IR		173	°C

Note:
1. FEA: Finite Element Analysis Method, IR: Infra-Red Method
2. Median Lifetime under pulsed condition is that under CW condition divided by duty cycle.

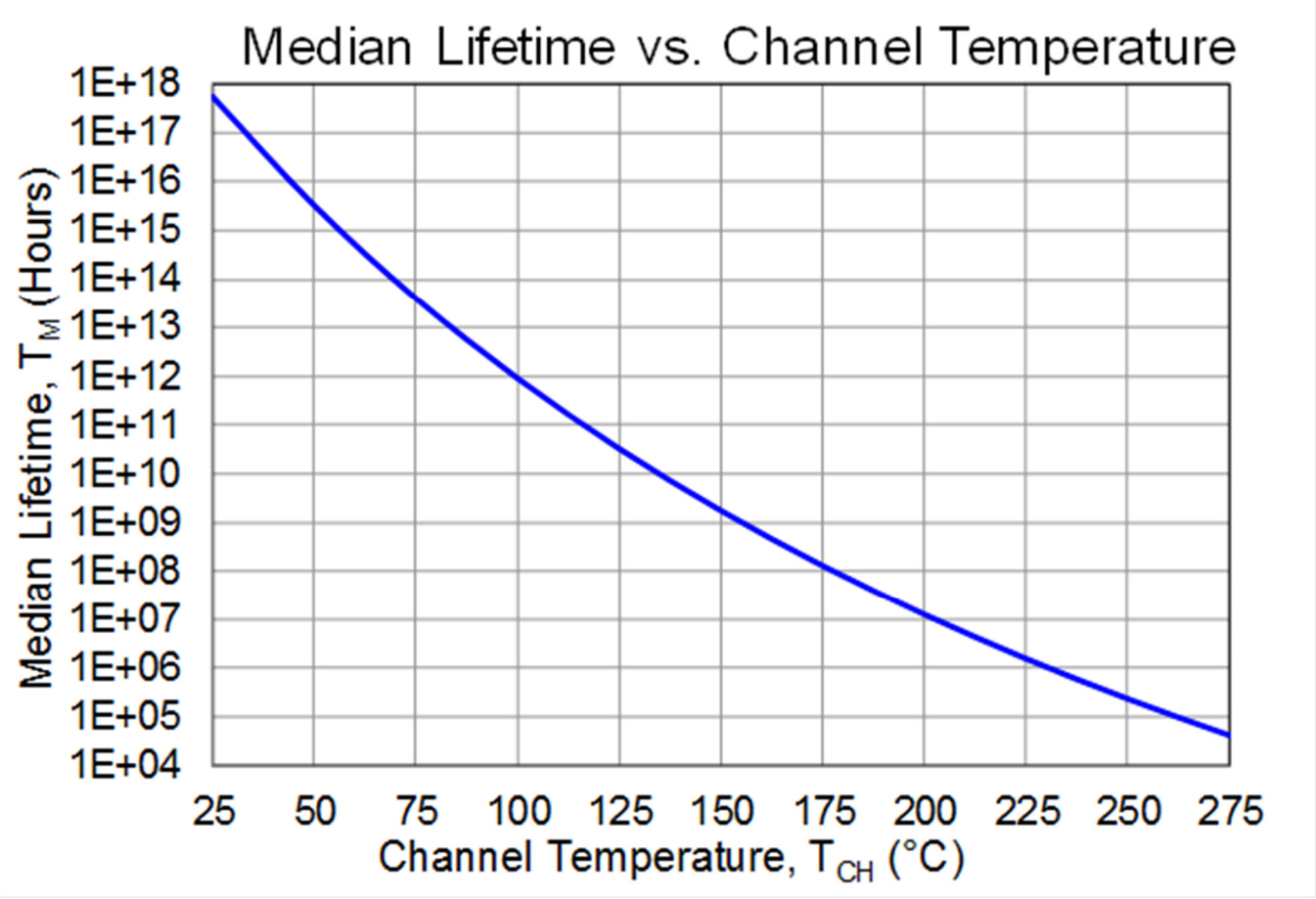
Thermal and Reliability Information – CW[1]



Parameter	Conditions	Values	Units
Thermal Resistance, FEA (θ_{JC})	85 °C Case 2.52 W Pdiss	17.9	°C/W
Peak Channel Temperature, FEA (T_{CH})		130	°C
Median Lifetime, FEA (T_M)[2]		2.7E10	Hrs
Peak Channel Temperature, IR		116	°C
Thermal Resistance, FEA (θ_{JC})	85 °C Case 3.78 W Pdiss	18.8	°C/W
Peak Channel Temperature, FEA (T_{CH})		156	°C
Median Lifetime, FEA (T_M)[2]		1.3E9	Hrs
Peak Channel Temperature, IR		133	°C
Thermal Resistance, FEA (θ_{JC})	85 °C Case 5.04 W Pdiss	19.8	°C/W
Peak Channel Temperature, FEA (T_{CH})		185	°C
Median Lifetime, FEA (T_M)[2]		6.5E7	Hrs
Peak Channel Temperature, IR		152	°C
Thermal Resistance, FEA (θ_{JC})	85 °C Case 6.30 W Pdiss	21.1	°C/W
Peak Channel Temperature, FEA (T_{CH})		218	°C
Median Lifetime, FEA (T_M)[2]		3.3E6	Hrs
Peak Channel Temperature, IR		171	°C

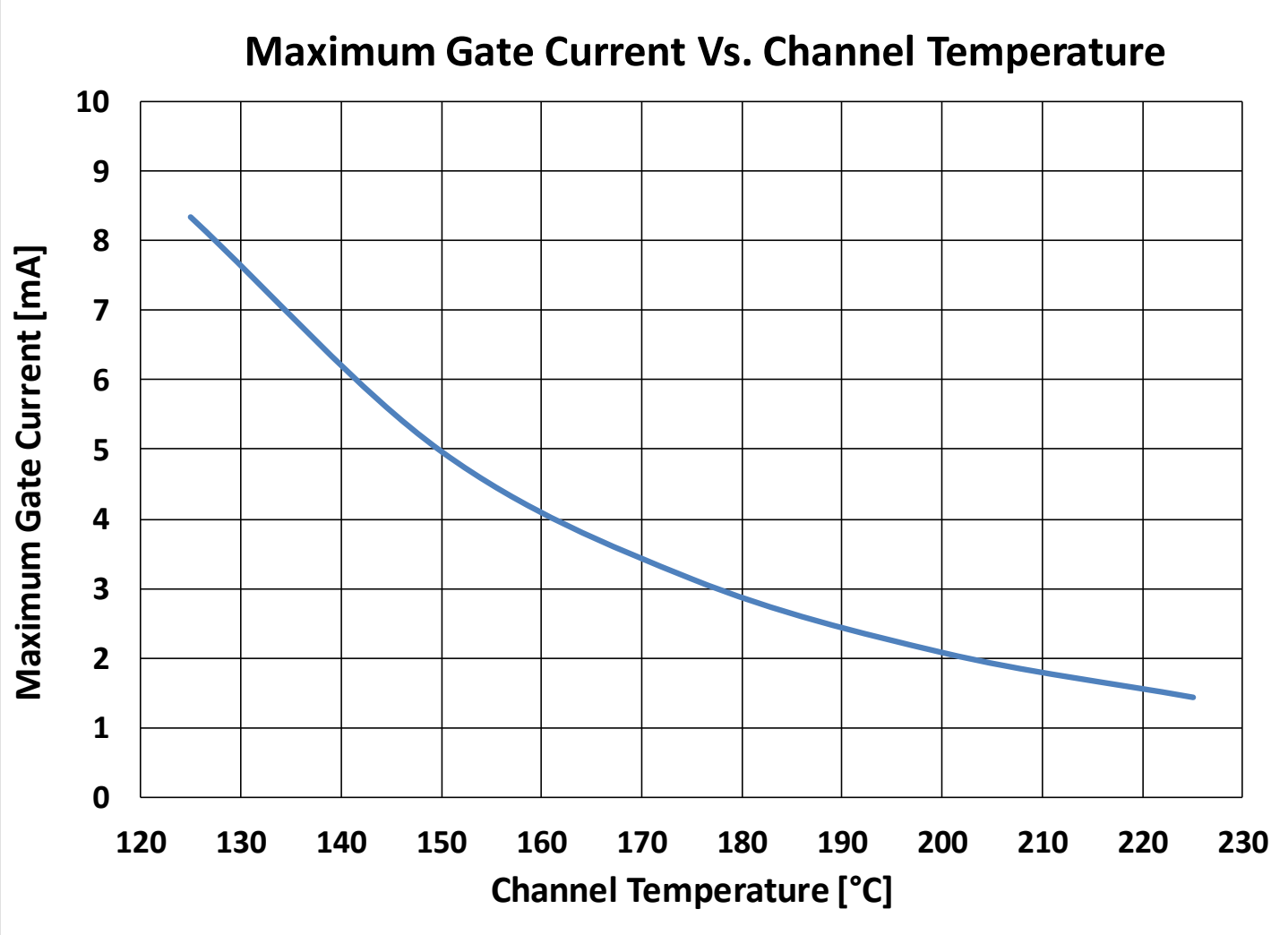
Note:
1. FEA: Finite Element Analysis Method, IR: Infra-Red Method

Median Lifetime[1]



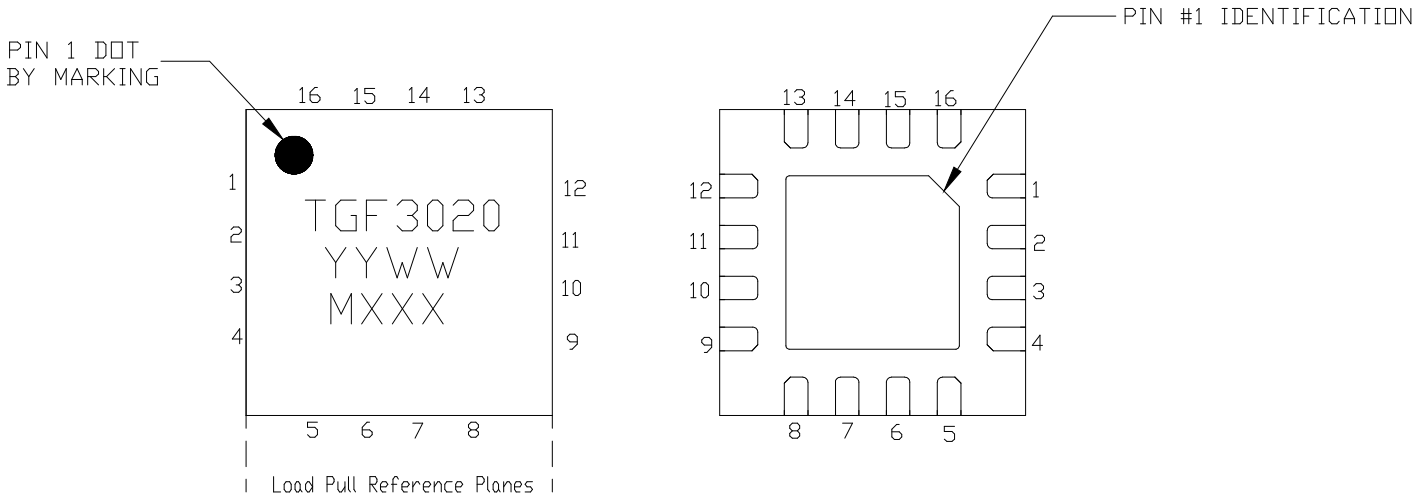
Notes:
1. Test Conditions: V_D = +32 V; Failure Criteria = 10 % reduction in I_{D_MAX} during DC Life Testing .

Maximum Gate Current



Pin Configuration and Description[1]

Note 1: The TGF3020-SM will be marked with the “TGF3020” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the MXXX” is the production lot number.



Pin	Symbol	Description
2, 3	RF IN / V_G	Gate
10, 11	RF OUT / V_D	Drain
1, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15, 16	NC	No Connection[1]
	Source	Source / Ground / Backside of part

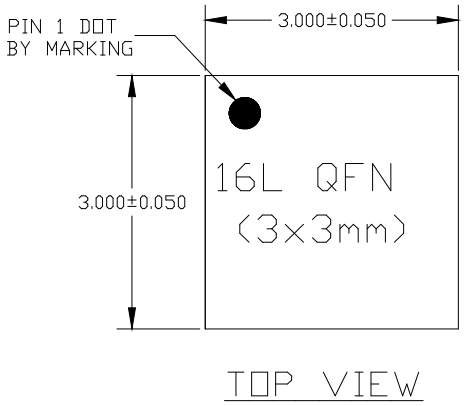
Note 1: Grounding pin 6 will cause performance degradation.

Mechanical Drawing[1]

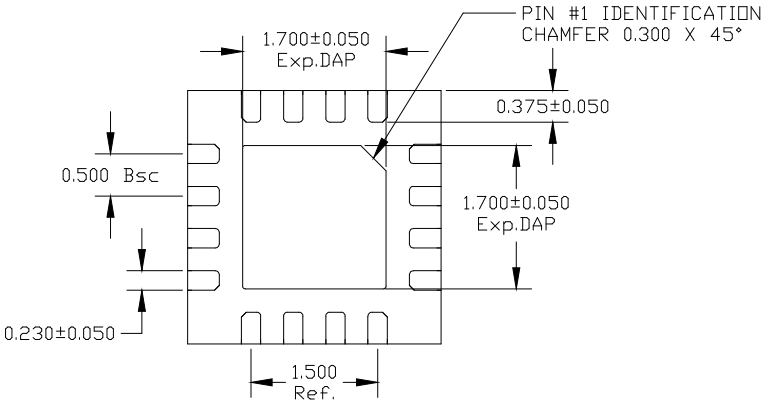
Note 1:

Unless otherwise noted, all dimention tolerances are +/-0.127 mm.

This package is lead-free/RoHS-compliant. The plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 ℃ reflow temperature) and tin-lead (maximum 245℃ reflow temperature) soldering processes.

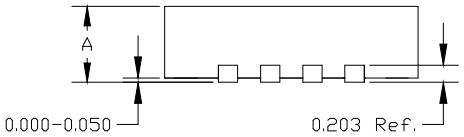


TOP VIEW



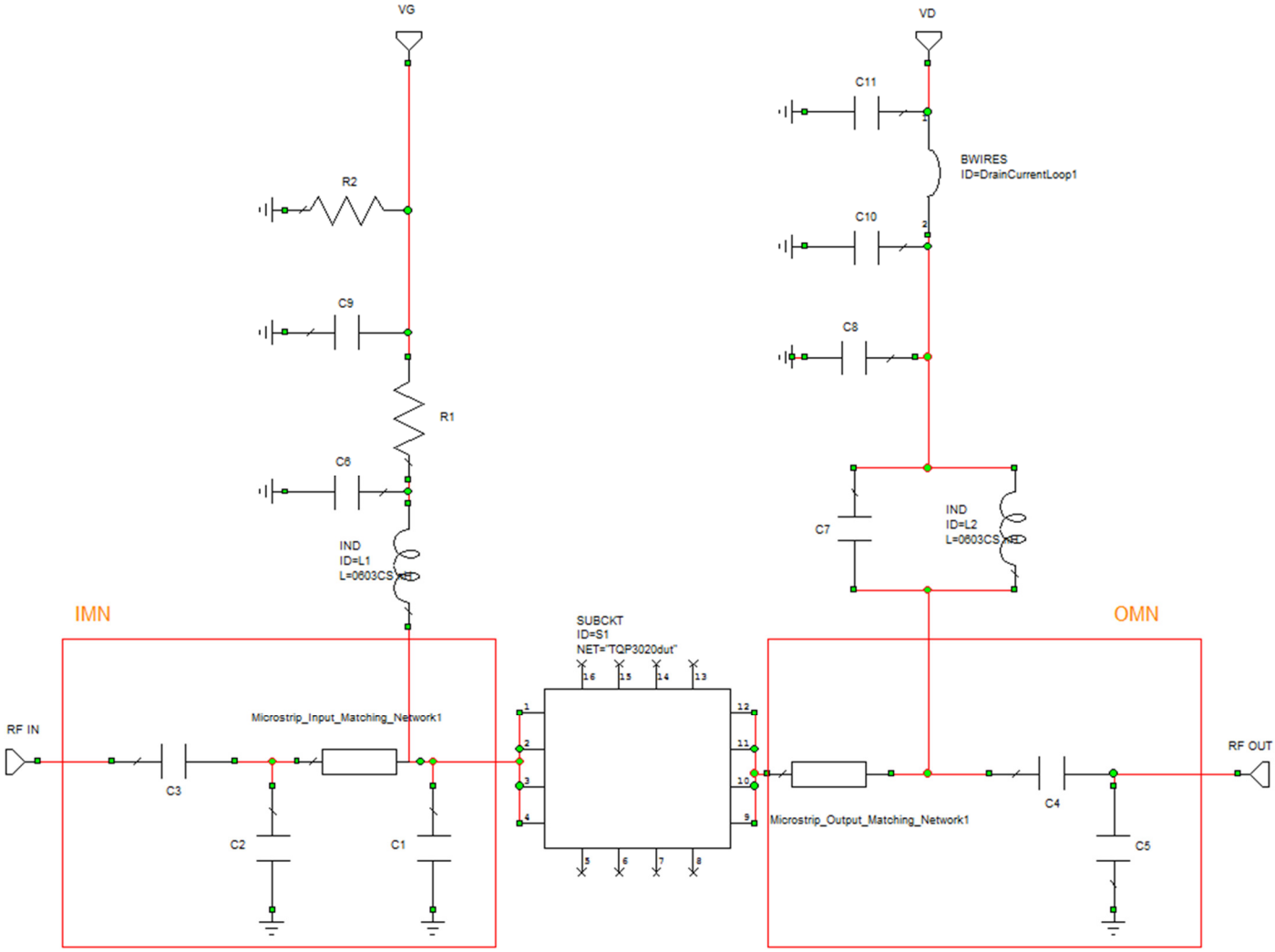
BOTTOM VIEW

		SLP
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800



TOP VIEW

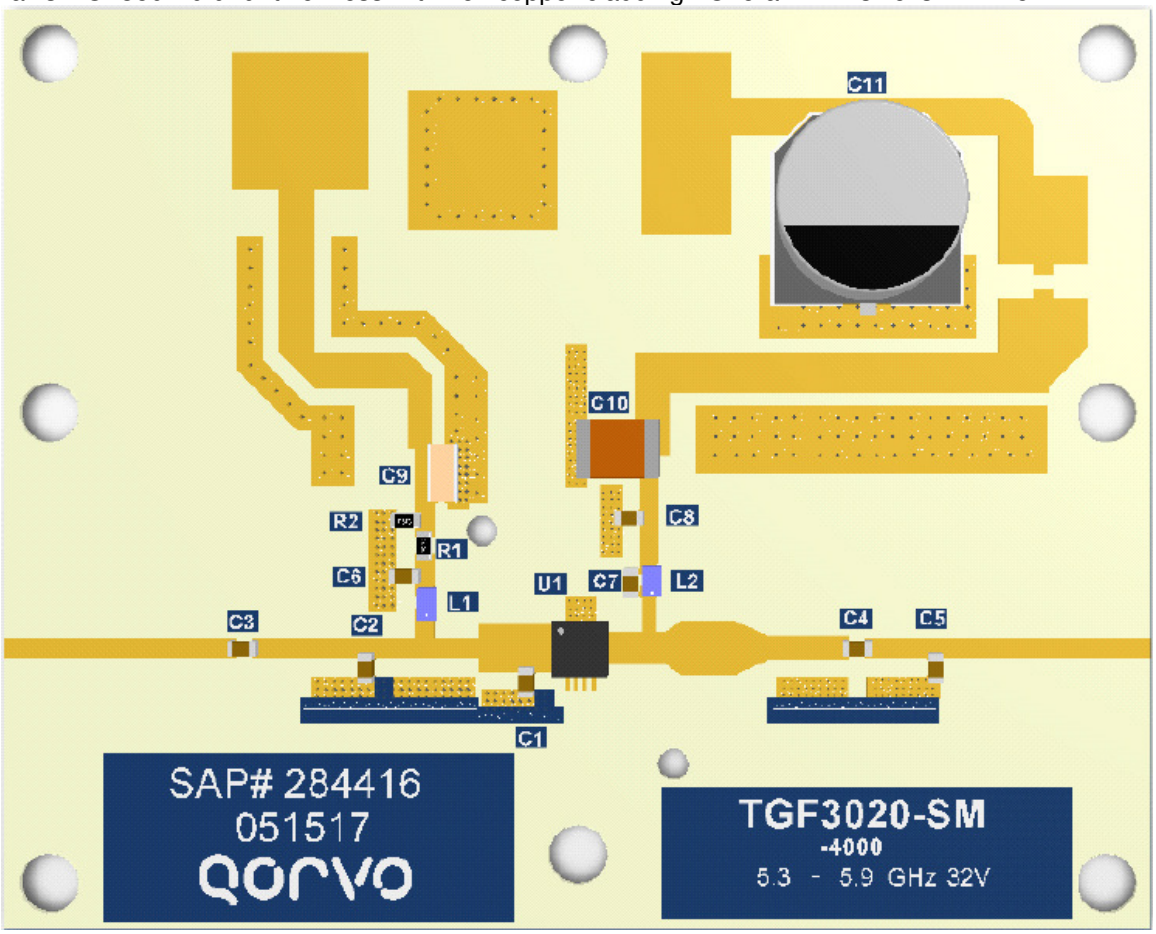
5.3 – 5.9 GHz Application Circuit - Schematic



Bias-up Procedure	Bias-down Procedure
1. Set V_G to -3.5 V.	1. Turn off RF signal.
2. Set I_D current limit to 30 mA.	2. Turn off V_D
3. Apply 32 V V_D.	3. Wait 2 seconds to allow drain capacitor to discharge.
4. Slowly adjust V_G until I_D is set to 25 mA.	4. Turn off V_G
5. Set I_D current limit to 0.3 A (Pulsed operation.)	
6. Apply RF.	

3.1 – 3.5 GHz Application Circuit - Layout

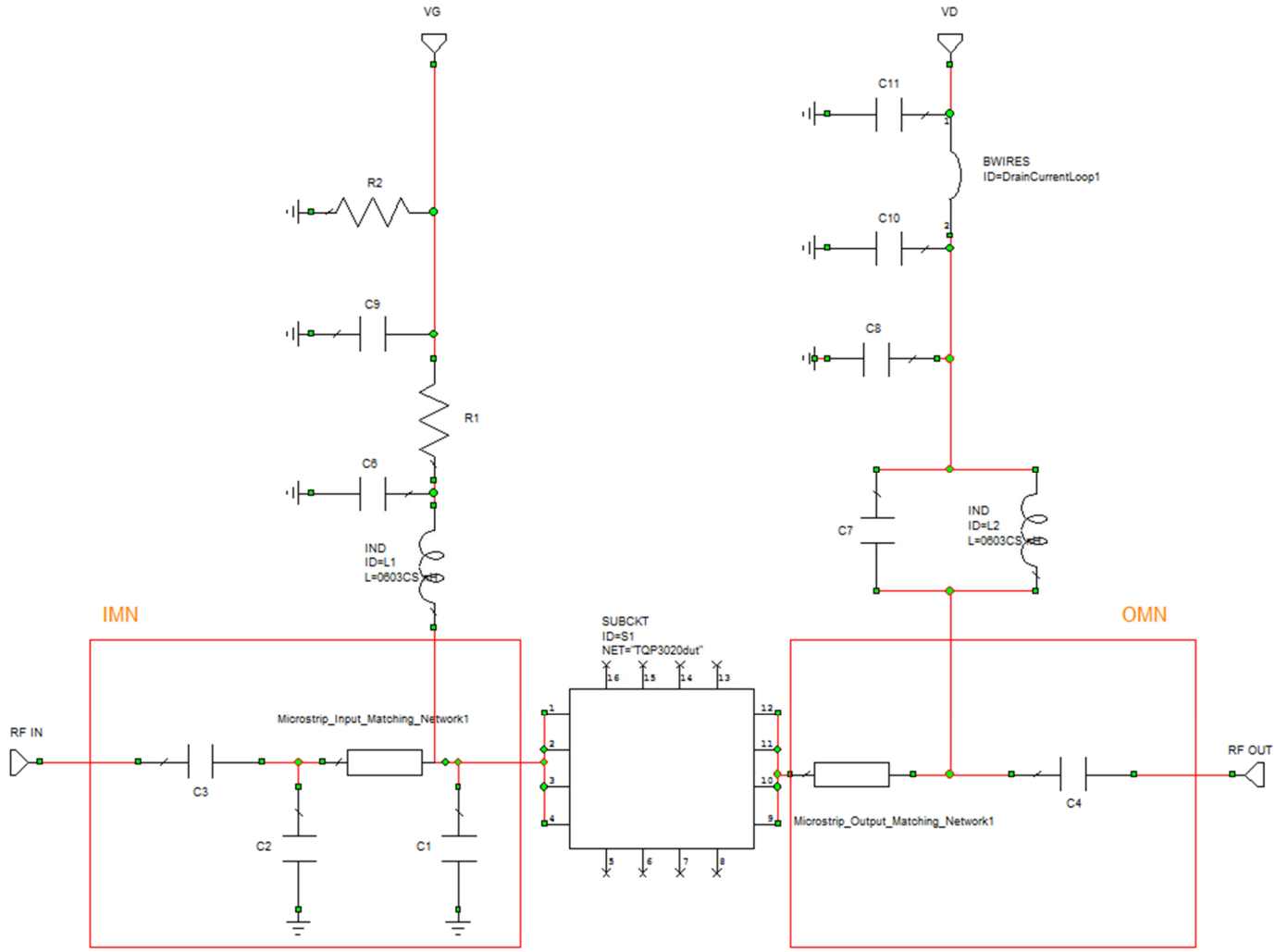
Board material is RO4350B 0.020” thickness with 1oz copper cladding. Overall EVB size is 2” x 2.5”.



3.1 – 3.5 GHz Application Circuit - Bill of Materials

Reference Design	Value	Qty	Manufacturer	Part Number
R1	10 Ω	1		Generic 0603
R2	1 kΩ	1		Generic 0603
C1, C5	0.2 pF	2	PPI	0603N0R2AW251X
C2	0.3 pF	1	PPI	0603N0R3AW251X
C3, C4	5.1 pF	2	PPI	0603N5R1AW251X
C6, C7, C8	3.3 pF	3	PPI	0603N3R3AW251X
C11	220 uF	1	United Chemicon	EMVY500ADA221MJA0G
C9	10 uF	1	TDK	C1632X5R0J106M130AC
C10	1 uF	1	AVX	18121C105KAT2A
L1	3.9nH	1	CoilCraft	0603CS-3N9X_E
L2	2.2nH	1	CoilCraft	0603CS-2N2X_E

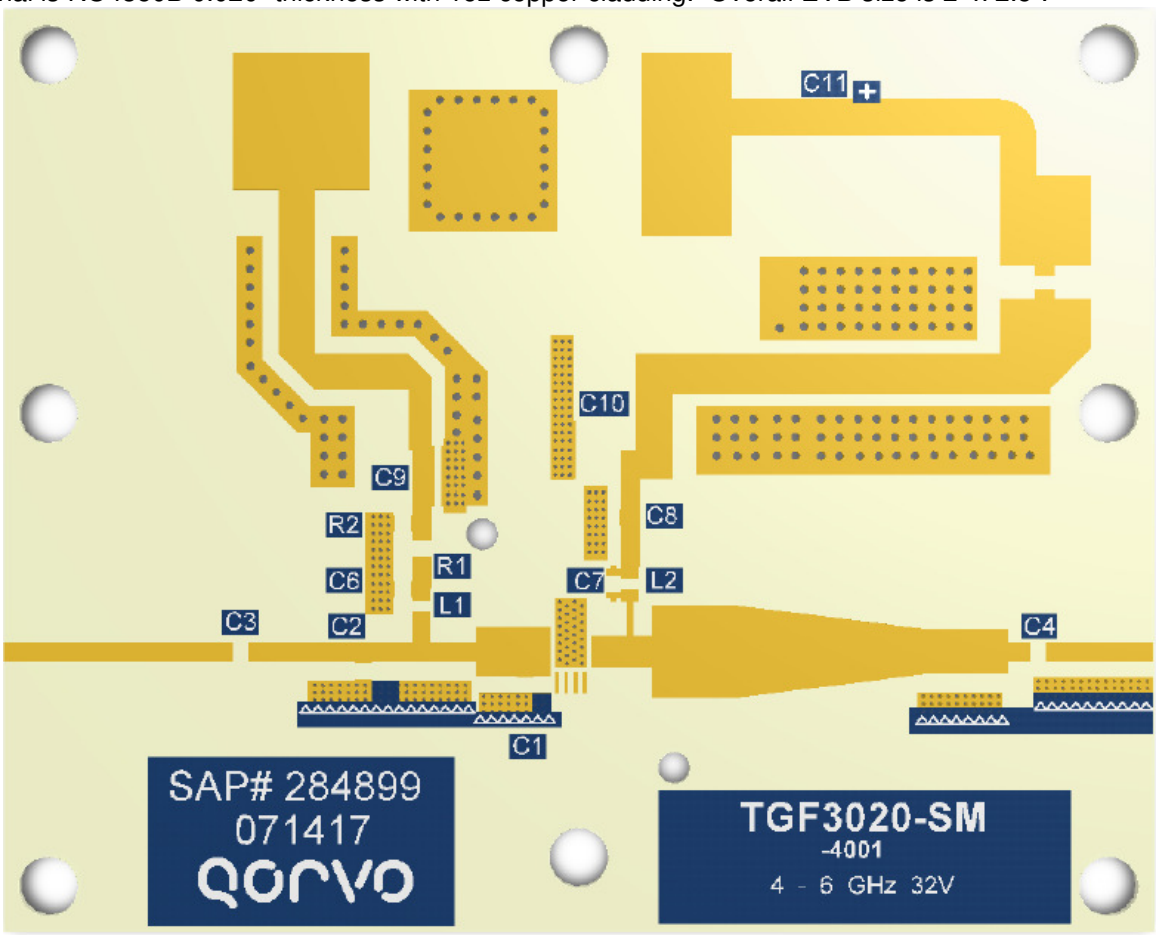
4 – 6 GHz Application Circuit - Schematic



Bias-up Procedure	Bias-down Procedure
2. Set V_G to -4 V.	3. Turn off RF signal.
4. Set I_D current limit to 30 mA.	4. Turn off V_D
5. Apply 32 V V_D.	5. Wait 2 seconds to allow drain capacitor to discharge.
6. Slowly adjust V_G until I_D is set to 25 mA.	7. Turn off V_G
8. Set I_D current limit to 0.3 A (Pulsed operation.)	
9. Apply RF.	

4 – 6 GHz Application Circuit - Layout

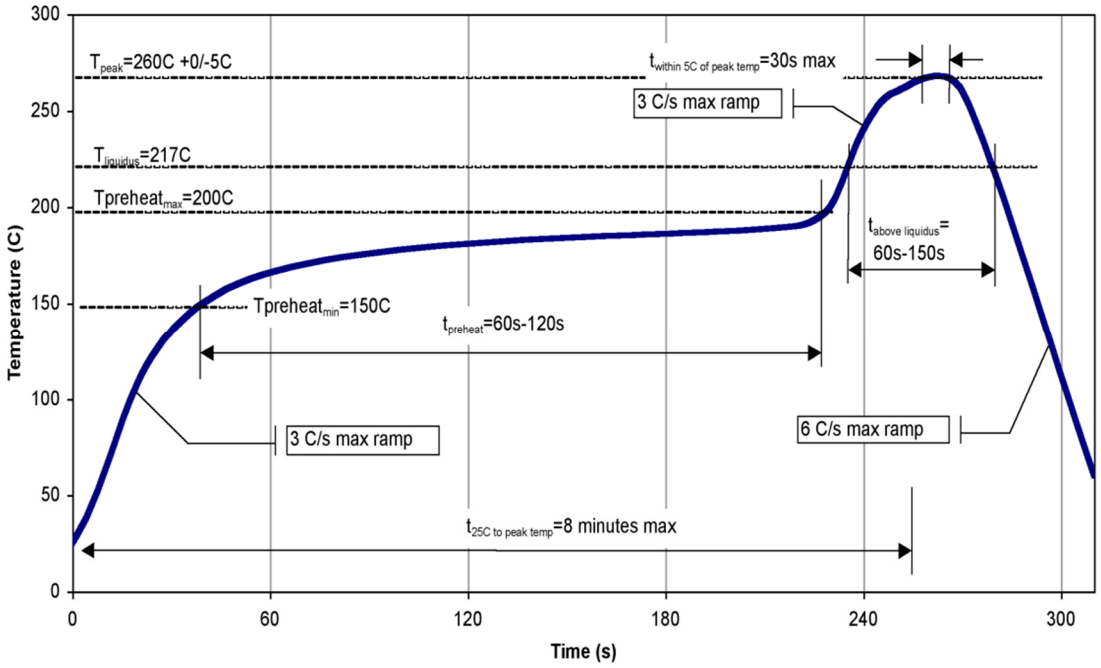
Board material is RO4350B 0.020” thickness with 1oz copper cladding. Overall EVB size is 2” x 2.5”.



4 – 6 GHz Application Circuit - Bill of Materials

Reference Design	Value	Qty	Manufacturer	Part Number
R1	10 Ω	1		Generic 0603
R2	1 kΩ	1		Generic 0603
C1	0.2 pF	1	PPI	0603N0R2AW251X
C2	0.3 pF	1	PPI	0603N0R3AW251X
C3	5.1 pF	1	PPI	0603N5R1AW251X
C4	10 pF	1	PPI	0603N100AW251X
C6, C7, C8	3.3 pF	3	PPI	0603N3R3AW251X
C11	220 uF	1	United Chemicon	EMVY500ADA221MJA0G
C9	10 uF	1	TDK	C1632X5R0J106M130AC
C10	1 uF	1	AVX	18121C105KAT2A
L1	3.9nH	1	CoilCraft	0603CS-3N9X_E
L2	1.8nH	1	CoilCraft	0603CS-1N8X_E

Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	3 @ 260°C	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

Web: www.Qorvo.com **Tel:** +1.972.994.8465
Email: info-sales@qorvo.com **Fax:** +1.972.994.8504

For technical questions and application information: **Email:** info-products@qorvo.com

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