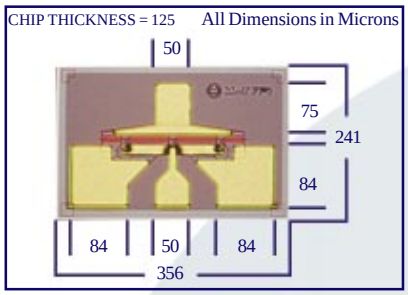
MwT-4

26 GHz Low Noise GaAs FET

DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



FEATURES

- 1.5 dB NOISE FIGURE AT 12 GHz
- HIGH ASSOCIATED GAIN
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 180 MICRON GATE WIDTH
- CHOICE OF CHIP AND TWO PACKAGE TYPES

DESCRIPTION

The MwT-4 is a GaAs MESFET device whose nominal quarter-micron gate length and 180 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 26 GHz frequency range. The straight geometry of the MwT-4 makes it equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal system and devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability, Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

DC SPECIFICATIONS AT Ta = 25°C

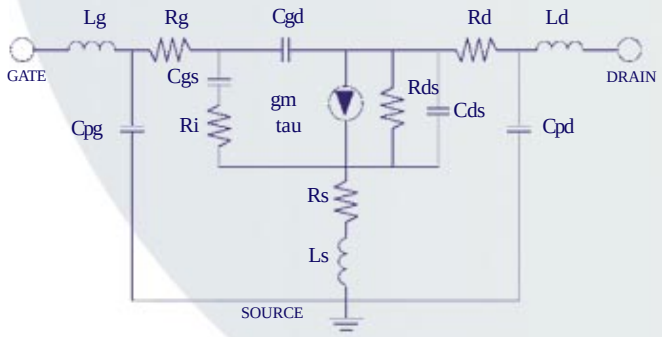
SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 4.0 V VGS= 0.0 V	mA	18		66
Gm	Transconductance Vds= 2.0 V VGS= 0.0 V	mS	27	35	
Vp	Pinch-off Voltage Vds= 3.0 V IDS= 5.0 mA	V		-1.5	-4.0
BVGSO	Gate-to-Source Breakdown Volt. Igs= -1.0 mA	V	-5.0	-8.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= -1.0 mA	V	-6.0	-8.0	
Rth	Thermal Resistance MwT-4 Chip, MwT-470, 473	°C/W			250 460*

*Overall Rth depends on case mounting.

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 4.5 V IDS= 0.6 x IDSS	12 GHz	dBm	13.0	14.0
SSG	Small Signal Gain VDS= 4.5 V IDS= 0.6 x IDSS	12 GHz	dB	8.0	9.0
NFopt	Optimum Noise Figure VDS= 3.0V IDS= 10mA	12 GHz	dB		1.5
GA	Gain at Optimum Noise Figure VDS= 3.0V IDS= 10mA	12 GHz	dB	8.0	9.0
IDSS	Recommended IDSS Range for Optimum P1dB		mA		24-51

DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER		VALUE	
Source Resistance	Rs	4.08	Ω
Source Inductance	Ls	0.03	nH
Drain-Source Resistance	Rds	283	Ω
Drain-Source Capacitance	Cds	0.054	pF
Drain Resistance	Rd	6.99	Ω
Drain Pad Capacitance	Cpd	0.04	pF
Drain Inductance	Ld	0.27	nH
Gate Bond Wire Inductance	Lg	0.11	nH
Gate Pad Capacitance	Cpg	0.07	pF
Gate Resistance	Rg	0.13	Ω
Gate-Source Capacitance	Cgs	0.22	pF
Channel Resistance	Ri	10.8	Ω
Gate-Drain Capacitance	Cgd	0.02	pF
Transconductance	gm	44.0	mS
Transit Time	tau	2.66	psec

ORDERING INFORMATION

Chip	MwT-4
Package 71	MwT-471
Package 73	MwT-473

NOTE:
For Package information, please see supplimentary application note from our website at www.mwtinc.com. When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

4268 Solar Way Fremont California 94538 Phone: (510) 651-6700 Fax: (510) 651-2208

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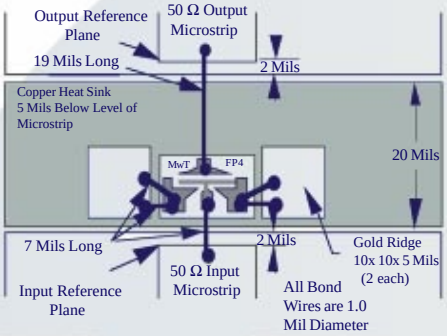
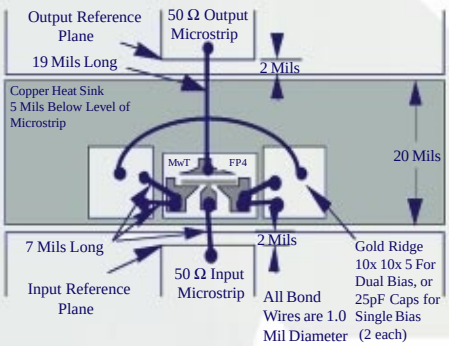
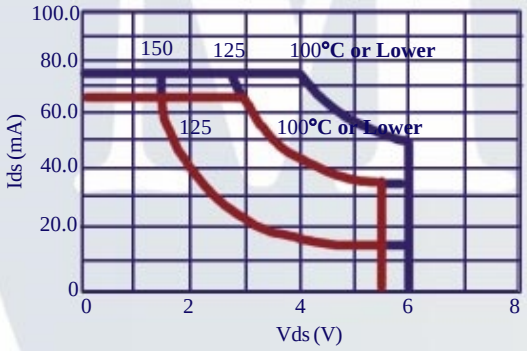
MwT-4
DUAL BIAS



MwT-4
OPTIONAL BONDING



SAFE OPERATING LIMITS vs. BACKSIDE CHIP



Absolute Maximum Continuous Maximum

MAXIMUM RATINGS AT Ta = 25°C

SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	55	85

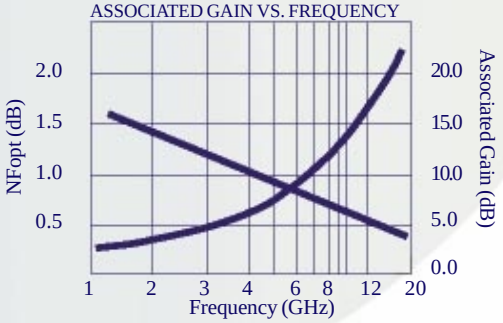
NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

TYPICAL NOISE PARAMETERS

MwT-4LN Chip: VDS= 3.0V IDS= 10mA

FREQUENCY GHz	NF MIN dB	GAMMA OPT MAG	GAMMA OPT ANGLE	Rn/50
1.00	0.38	0.95	4.5	0.94
2.00	0.4	0.9	15.5	0.83
4.00	0.64	0.76	31.4	0.53
6.00	0.86	0.64	48	0.43
8.00	1.07	0.54	66.1	0.38
12.00	1.47	0.42	107.1	0.32
16.00	1.83	0.4	148.7	0.29
18.00	2.0	0.42	166.4	0.28
20.00	2.16	0.46	-178.5	0.26

NOISE FIGURE AND
ASSOCIATED GAIN VS. FREQUENCY



MwT-4	Bin	A	B	C	D
	Idss Range	18-24	24-33	33-51	51-60

BIN ACCURACY STATEMENT

When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

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