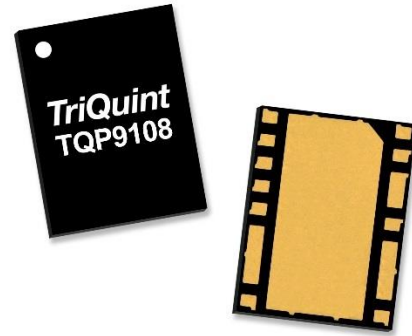


General Description

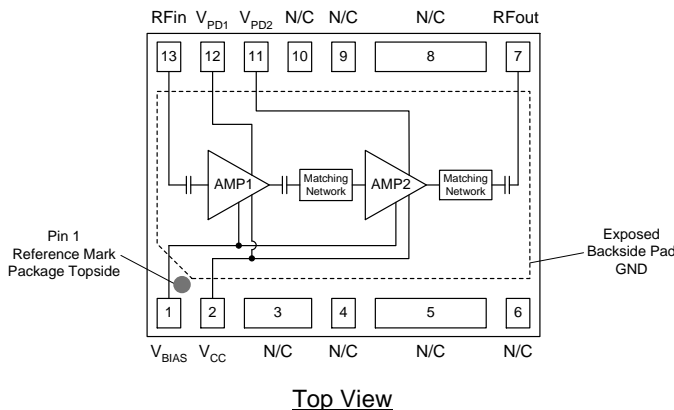
The TQP9108 is a high-efficiency two-stage power amplifier in a low-cost surface-mount package. The amplifier is able to achieve 39% power added efficiency at +27 dBm output power while operating with a low 65 mA idle current. The amplifier is designed to ensure that all odd-order IMD products are below -17 dBm at all output power levels below +24 dBm/tone.

The TQP9108 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The TQP9108 is available in a lead-free/RoHS-compliant 13-pin 3.5 x 4.5mm surface mount package and is pin-compatible to the higher frequency band version in the family with the TQP9107 (699-960 MHz).



3.5 x 4.5 mm Leadless SMT Package

Functional Block Diagram



Product Features

- 1.71 – 2.17 GHz Frequency Range
- 30.5 dB gain
- +46 dBm Output IP3 at Pout = +24 dBm/tone
- 39% PAE at +27 dBm Pout
- Internally Matched
- Integrated Inter-Stage Matching
- Bias Adjustable
- Low idle current

Applications

- Wireless Infrastructure
- Repeaters, Boosters, DAS
- High Power Amplifiers
- Small cell BTS

Ordering Information

Part No.	Description
TQP9108	1.71 – 2.17 GHz Power Amplifier
TQP9108-PCB	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to +150 °C
RF Input Power, CW, 50 Ω, T=25 °C	+12 dBm
Supply Voltage (V _{CC})	+6 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{CC}		+4.3	+5.0	V
V _{BIAS}		+4.0	V _{CC}	V
V _{PD1} , V _{PD2}		+4.0	V _{CC}	V
T _{CASE}	-40		+105	°C
T _j for >10 ⁶ hours MTTF			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

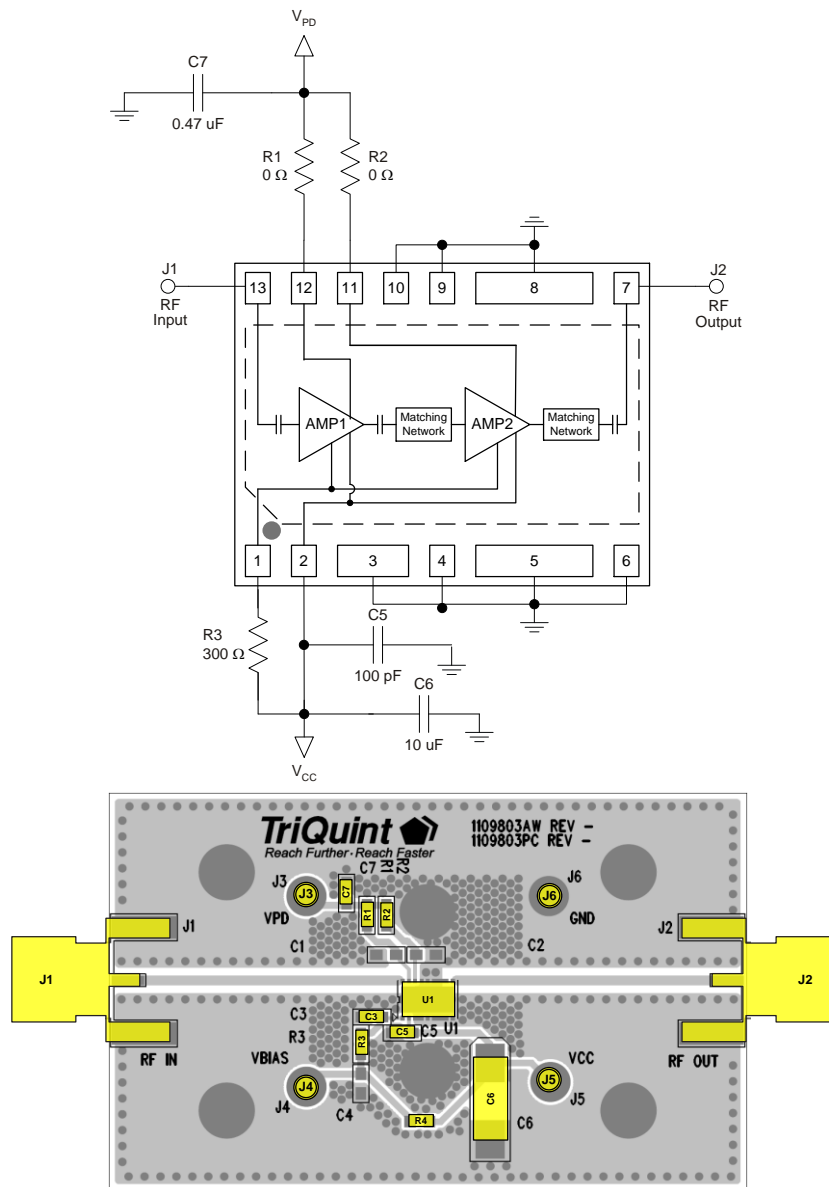
Electrical Specifications

Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Operational Frequency Range		1710		2170	MHz
Test Frequency			1915		MHz
Gain		28.8	30.5		dB
Noise Figure			5		dB
Output P1dB			+31.3		dBm
Output IP3	P _{out} = +23 dBm/tone, Δf = 600 kHz	+43	+46		dBm
IMD3, IMD5, IMD7	All power levels ≤ 23 dBm / tone			-17	dBm
Current, I _{CC}	P _{out} = +27 dBm		300		mA
Power Added Efficiency	P _{out} = +27 dBm		39		%
Idle Current	No RF Input Power		67		mA
VSWR Survivability	P _{out} = P1dB Signal: CW All Phases	10:1			–
VSWR Survivability	P _{out} = +28 dBm Signal: 20 MHz LTE 1C, PAR = 9.5 dB All Phases	6:1			–
Thermal Resistance, θ _{JC}	Junction to case		37.5		°C/W

Notes:

1. Test conditions unless otherwise noted: V_{CC} = +4.3 V, V_{PD1} = V_{PD2} = +4.0 V, Temp = +25 °C, 50 Ω system.

Application Circuit Schematic and Layout – TQP9108-PCB



Bill of Material – TQP9108-PCB

Reference Des.	Value	Description	Manuf.	Part Number
n/a		Nelco FR4, PCB APP BOARD	Qorvo	1109803PC
U1		2-Stage Power Amplifier	Qorvo	TQP9108
C5	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C6	10 uF	CAP, 6032, 20%, 50V, Tantalum	various	
C7	0.1 uF	CAP, 0603, 50V, X7R, 5%	various	
R1, R2, R4	0 Ω	RES, 0603, 5%, 1/16W, Chip	various	
R3	300 Ω	RES, 0603, 5%, 1/16W, Chip	various	

Typical Performance – TQP9108-PCB

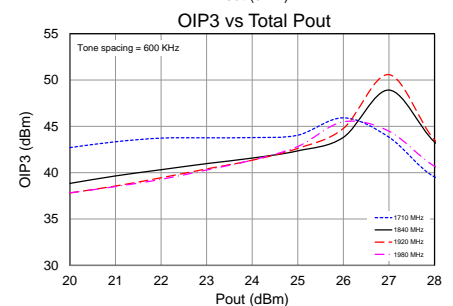
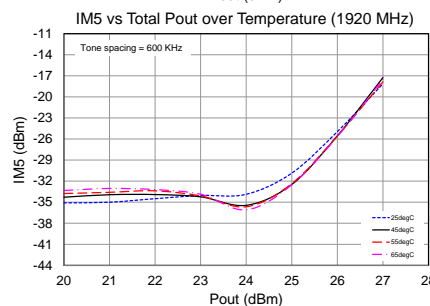
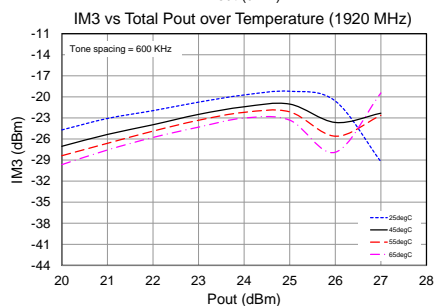
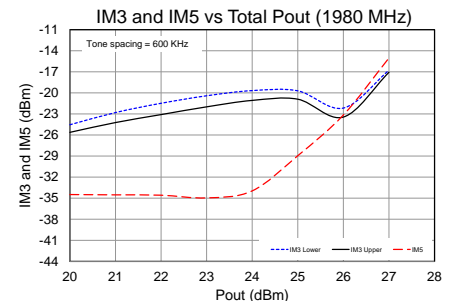
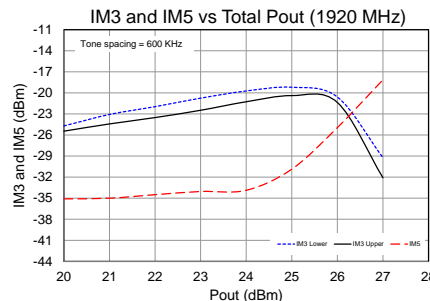
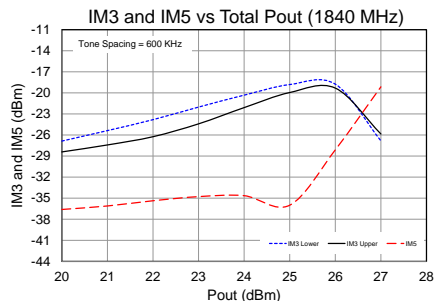
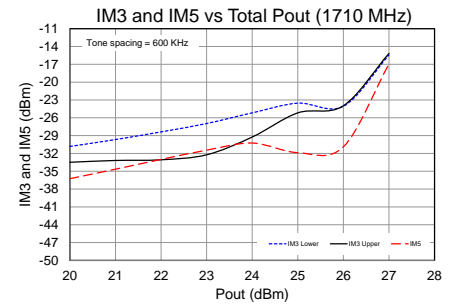
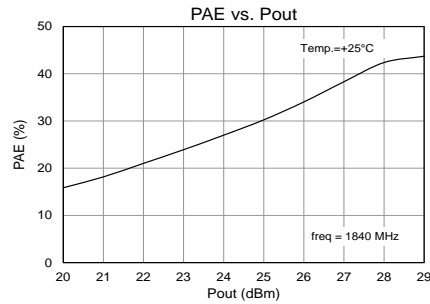
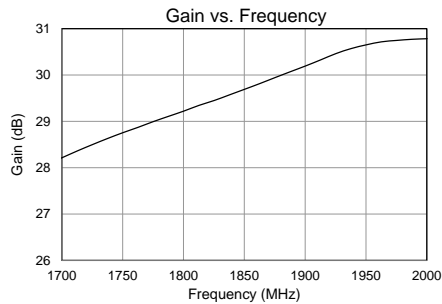
Parameter	Conditions ⁽¹⁾	Typical Value				Units
Frequency		1710	1840	1920	1980	MHz
Gain		28.4	29.6	30.4	30.7	dB
IM3	Pout= +27 dBm, Δf= 600 KHz	-15.5	-26	-29	-17	dBm
IM5	Pout= +27 dBm, Δf= 600 KHz	-17	-19	-18	-15.5	dBm
Quiescent Collector Current, I _{CQ}	V _{PD} = +4 V	67				mA

Notes:

1. Test conditions unless otherwise noted: V_{CC} = +4.3V, V_{PD1} = V_{PD2} = +4.0V, Temp.=+25 °C

Performance Plots – TQP9108-PCB

Test conditions unless otherwise noted: V_{CC} = +4.3V, V_{PD1} = V_{PD2} = +4.0V, Temp.=+25 °C



Typical Performance – $V_{CC} = +5.0\text{ V}$

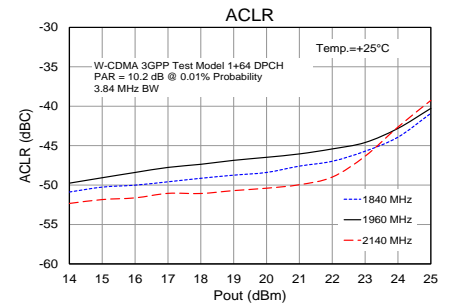
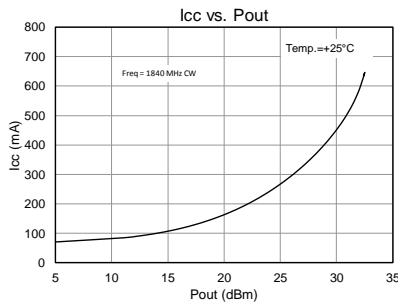
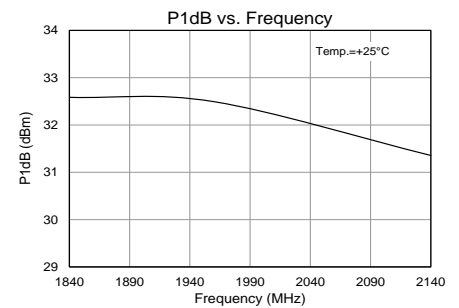
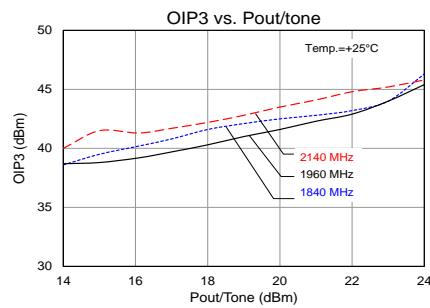
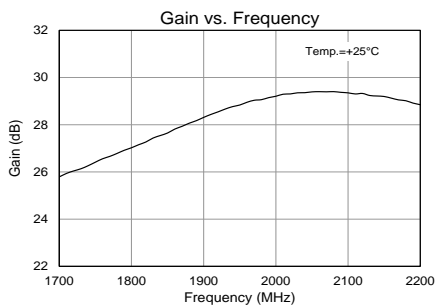
Parameter	Conditions ⁽¹⁾	Typical Value			Units
Frequency		1840	1960	2140	MHz
Gain		28	28.5	29.4	dB
Input Return Loss		-12	-11	-9	dB
Output P1dB		+32.6	+32.5	+31.4	dBm
Output IP3	Pout= +24 dBm, $\square f = 1\text{ MHz}$	+46.2	+45.4	+45.7	dBm
Quiescent Collector Current, I_{CQ}	$V_{PD} = +4.3\text{ V}$	84			mA

Notes:

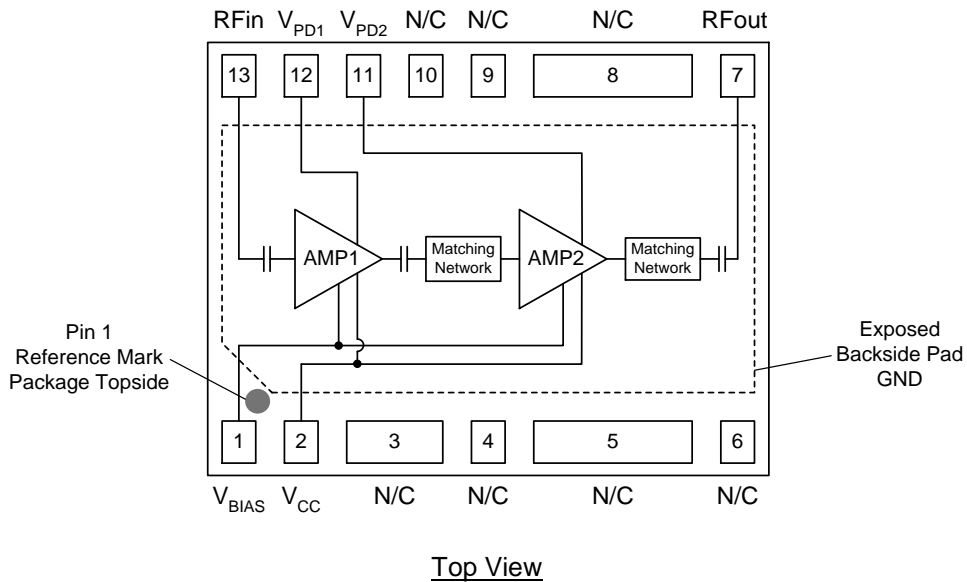
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Performance Plots – $V_{CC} = +5.0\text{ V}$

Test conditions unless otherwise noted: $V_{CC} = +5.0\text{ V}$, $V_{PD1} = V_{PD2} = +4.3\text{ V}$, Temp.=+25 °C



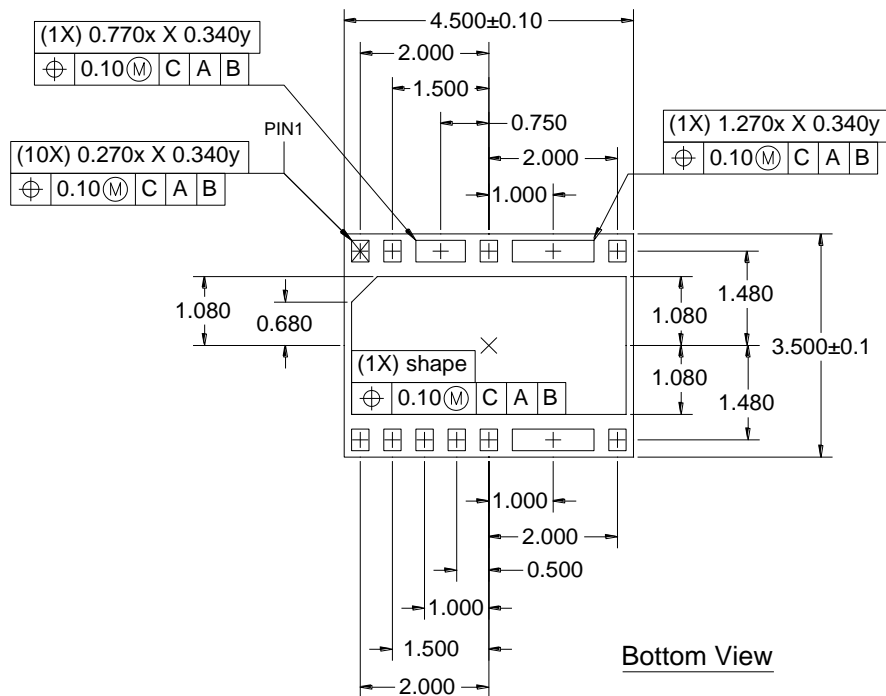
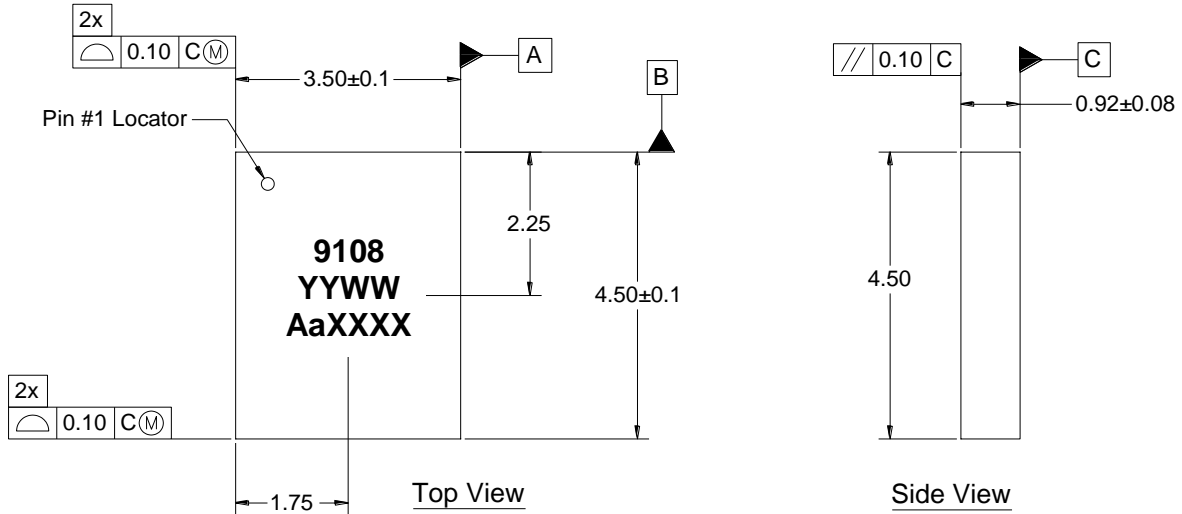
Pin Configuration and Description



Pad No.	Label	Description
1	V_{BIAS}	Provides reference voltage for internal active biasing circuit
2	V_{CC}	DC voltage supply connection
3, 4, 5, 6, 8, 9, 10	N/C	No internal connection. Provide grounded land pads for PCB mounting integrity.
7	RF out	RF output pin. The DC is internally blocked at this pin.
11	V_{PD1}	Power down for Amp 1. This voltage adjusts for the current draw in Amp 1.
12	V_{PD2}	Power down for Amp 2. This voltage adjusts for the current draw in Amp 2.
13	RF in	RF input pin. The DC is internally blocked at this pin.
Backside Pad	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Package Marking and Dimensions

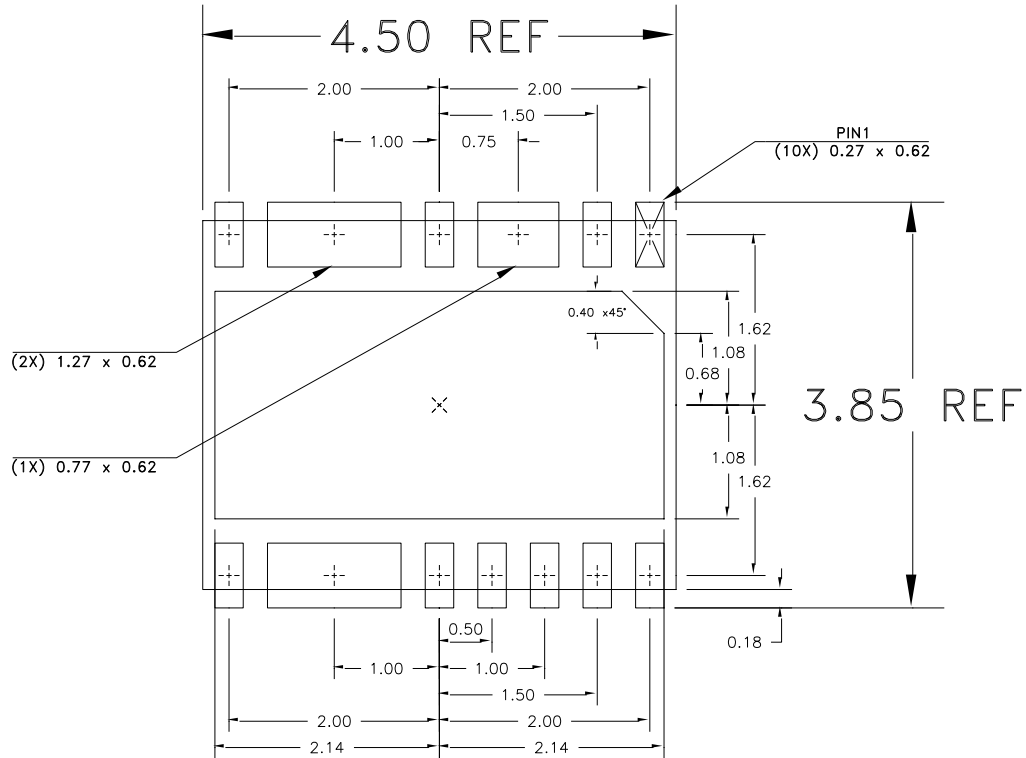
Marking: Part Number – TQP9108
 Date – YYWW
 Lot Code - AaXXXX



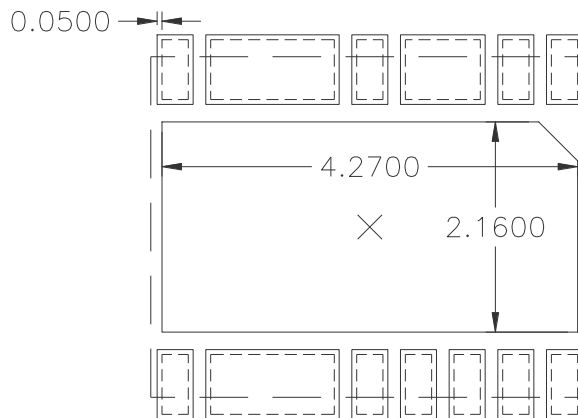
- Notes:
1. All dimensions are in millimeters. Angles are in degrees.
 2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
 3. Contact plating: Au over Ni

PCB Mounting Pattern

Recommend PCB land-pad pattern metallization (Top View)



Recommended PCB solder mask opening (Top View)



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.
Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment). This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free
- Qorvo Green



Contact Information

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Web: www.qorvo.com

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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