

Product Description

The Qorvo TGA4534-SM is a K-Band Power Amplifier with integrated power detector. The TGA4534-SM operates from 17.7 – 19.7 GHz and is designed using Qorvo’s power pHEMT production process.

The TGA4534-SM typically provides 34 dBm of saturated output power with small signal gain of 21 dB. Third Order Intercept is 42.5 dBm at 23 dBm SCL.

The TGA4534-SM is available in a low-cost, surface mount 28 lead 5x5 mm QFN package and is ideally suited for Point-to-Point Radio.

Lead-free and RoHS compliant



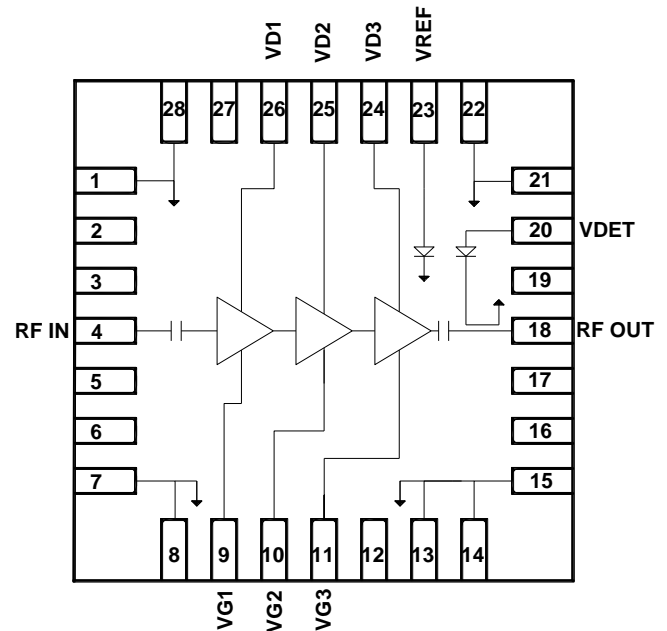
28 lead 5x5mm QFN package

Product Features

- Frequency Range: 17.7 – 19.7 GHz
- Power: 34 dBm Psat, 33 dBm P1dB
- Gain: 21 dB
- TOI: 42.5 dBm at 23 dBm/tone
- Integrated Power Detector
- Bias: Vd = 6 V, Idq = 1430 mA, Vg = -0.7 V Typical
- Package Dimensions: 5.0 x 5.0 x 1.3 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Point-to-Point Radio
- K-band Sat-Com

Ordering Information

Part	Description
TGA4534-SM	Waffle Tray
TGA4534-SM-T/R	500 pieces on a 7" reel (standard)
TGA4534-SM EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Drain to Gate Voltage, $V_D - V_G$	10 V
Drain Voltage (V_D)	6.5 V
Drain Current (I_D)	3.0 A
Gate Voltage Range (V_G)	-3 to 0 V
Gate Current (I_G)	-14 to +110 mA
Power Dissipation, P_{DISS}	20 W
RF Input Power, CW, $T = 25\text{ }^\circ\text{C}$	25 dBm
Channel Temperature, T_{CH}	200 $^\circ\text{C}$
Mounting Temperature (30 seconds)	260 $^\circ\text{C}$
Storage Temperature	-40 to 150 $^\circ\text{C}$

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage	6 V
Drain Current, Quiescent (I_{DQ})	1430 mA
Drain Current, RF (I_{DD_Drive})	See chart page 3
Gate Voltage, Typical Range (V_G)	-0.4 to -0.8 V
Gate Current, RF (I_{G_Drive}) Typical	40 mA
Operating Temperature Range	-40 to 85 $^\circ\text{C}$

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

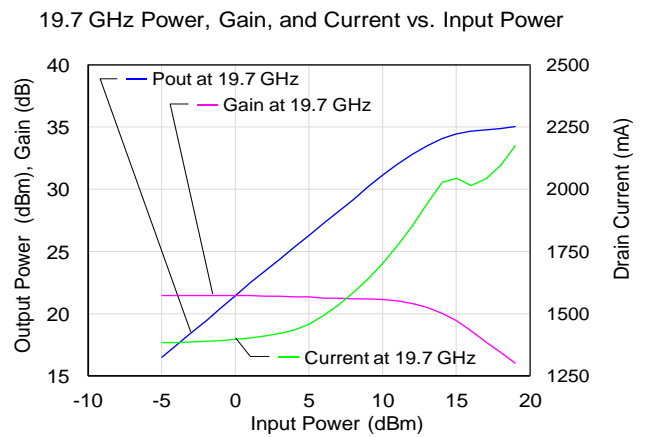
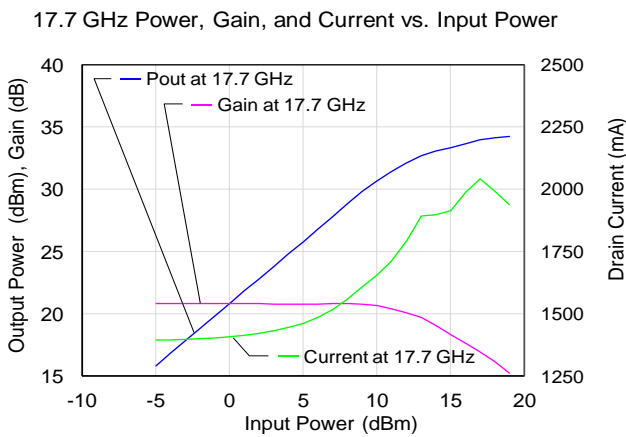
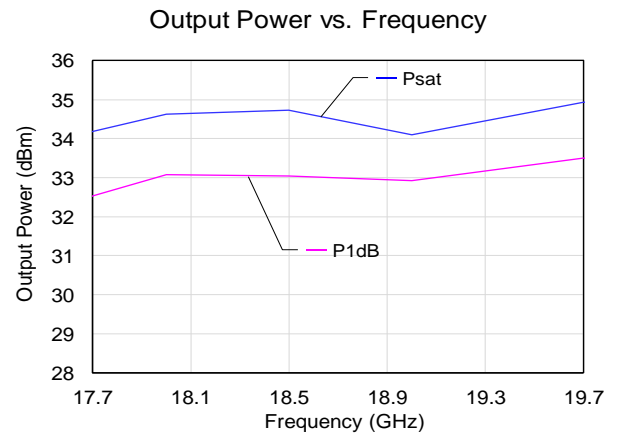
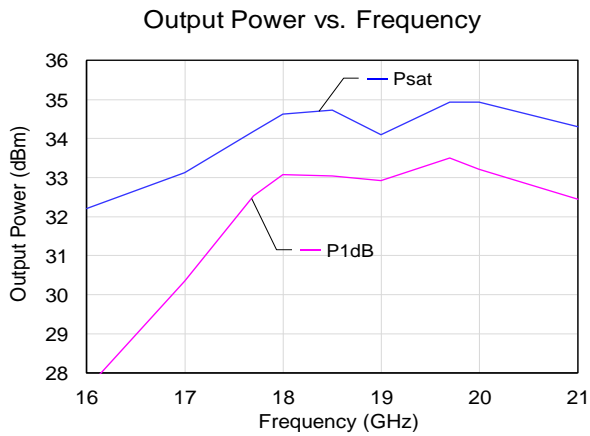
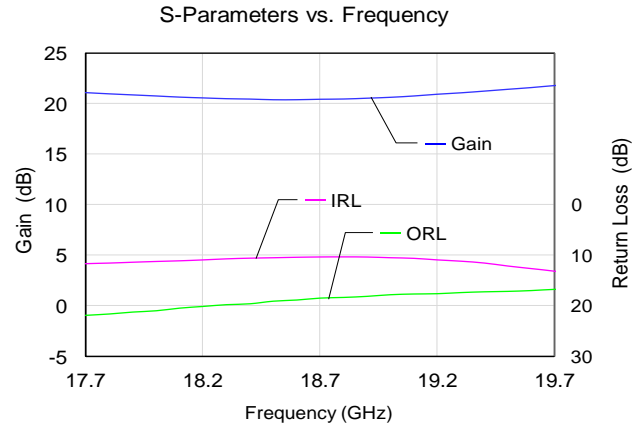
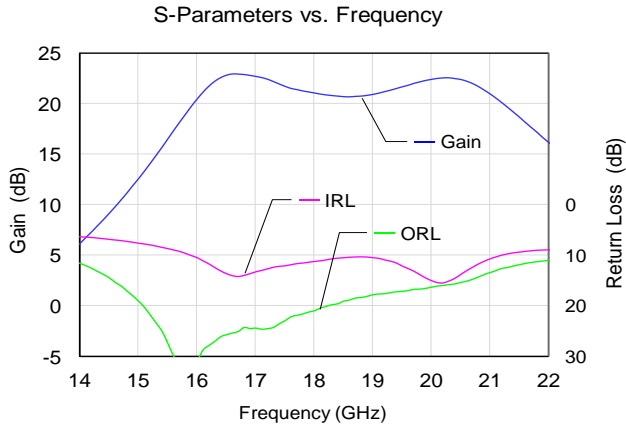
Electrical Specifications

Test conditions, unless otherwise noted: 25 $^\circ\text{C}$, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $V_G = -0.7\text{ V}$ typical, $Z_0 = 50\ \Omega$

Parameter	Min	Typical	Max	Units
Frequency	17.7		19.7	GHz
Small Signal Gain		21		dB
Input Return Loss		10		dB
Output Return Loss		12		dB
Output Power @ Saturation		34		dBm
Output Power @ 1 dB Gain Compression		33		dBm
Output TOI @ 23 dBm/Tone Pout/tone		42.5		dBm
Gain Temperature Coefficient		-0.02		dBm/ $^\circ\text{C}$
Power Temperature Coefficient		-0.005		dBm/ $^\circ\text{C}$

Performance Plots

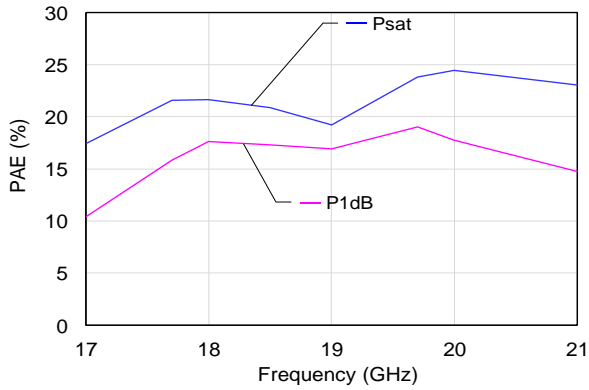
Test conditions unless otherwise noted: Temp. = 25 °C, $V_D = 6$ V, $I_{DQ} = 1430$ mA, $V_G = -0.7$ V typical



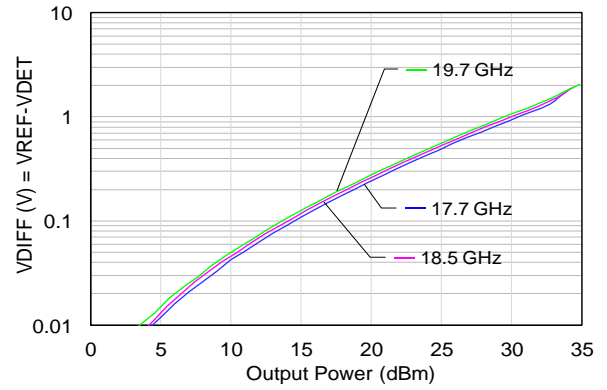
Performance Plots

Test conditions unless otherwise noted: Temp. = 25 °C, $V_D = 6$ V, $I_{DQ} = 1430$ mA, $V_G = -0.7$ V typical

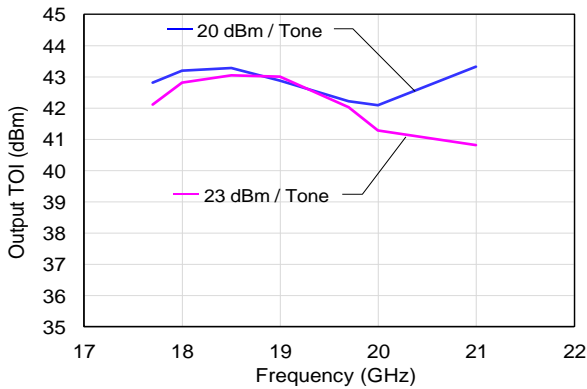
Power Added Efficiency vs. Frequency



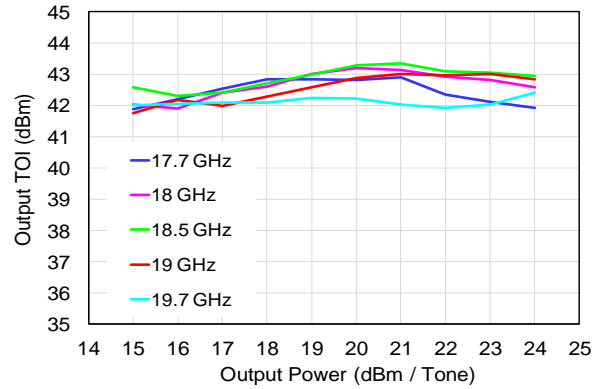
Power Detector vs. Output Power vs. Frequency



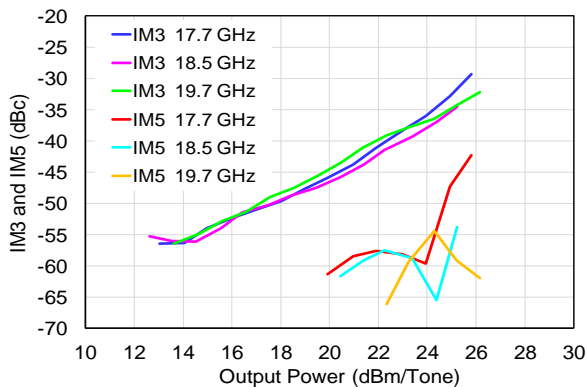
Output TOI vs. Frequency vs. Output Power / Tone



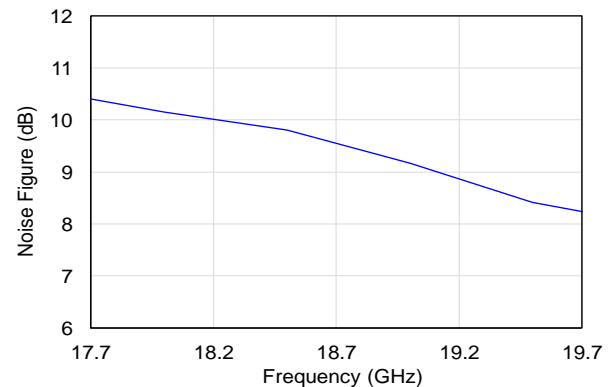
Output TOI vs. Output Power / Tone



IM3 and IM5 vs. Output Power / Tone vs. Frequency



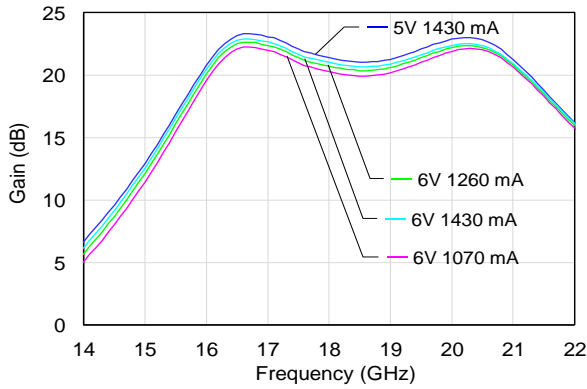
Noise Figure vs. Frequency



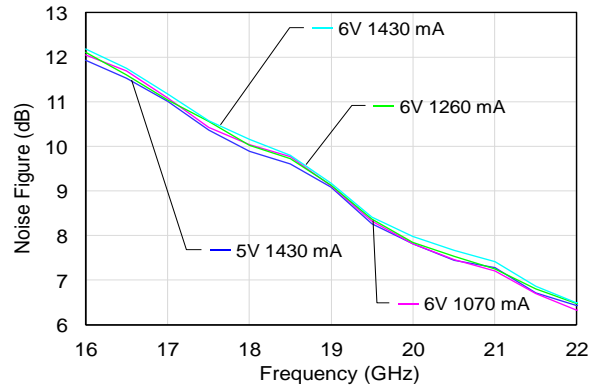
Performance Plots

Test conditions unless otherwise noted: Temp. = 25 °C, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $V_G = -0.7\text{ V}$ typical

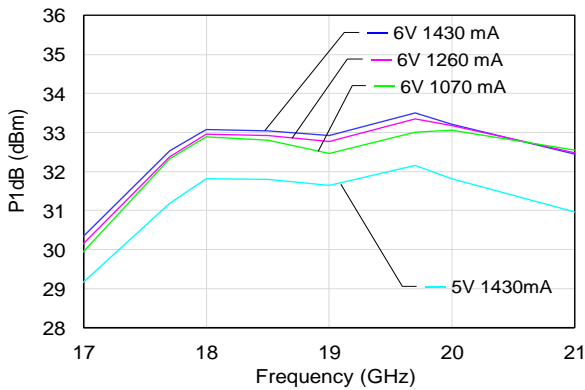
Gain vs. Frequency vs. Bias



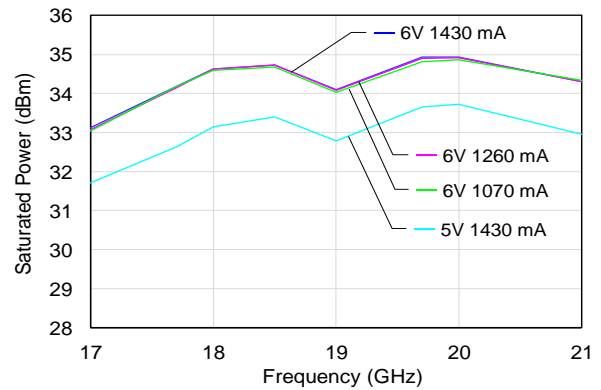
Noise Figure vs. Frequency vs. Bias



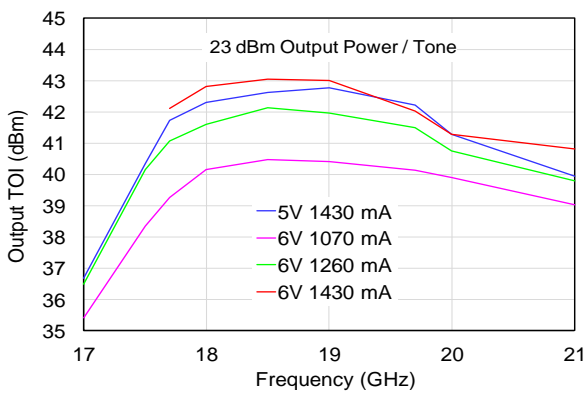
P1dB vs. Frequency vs. Bias



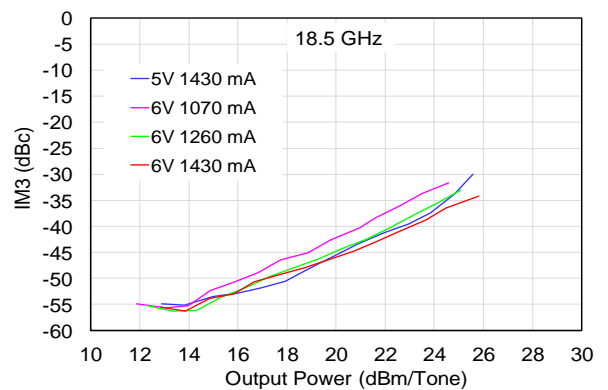
Saturated Power vs. Frequency vs. Bias



Output TOI vs. Frequency vs. Bias



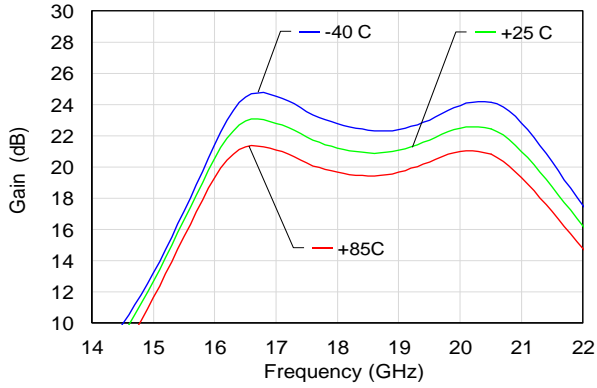
IM3 vs. Output Power / Tone vs. Bias



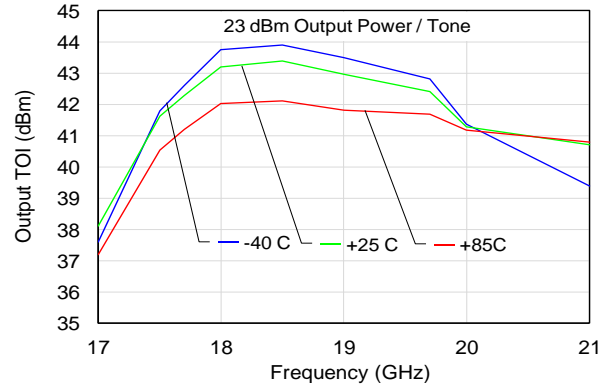
Performance Plots

Test conditions unless otherwise noted: Temp. = 25 °C, $V_D = 6\text{ V}$, $I_{DQ} = 1430\text{ mA}$, $V_G = -0.7\text{ V}$ typical

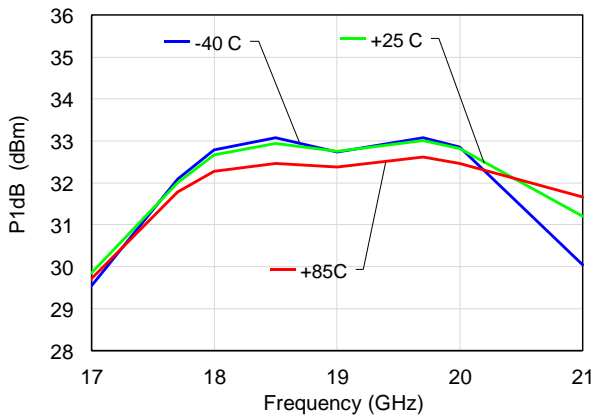
Gain vs. Frequency vs. Temperature



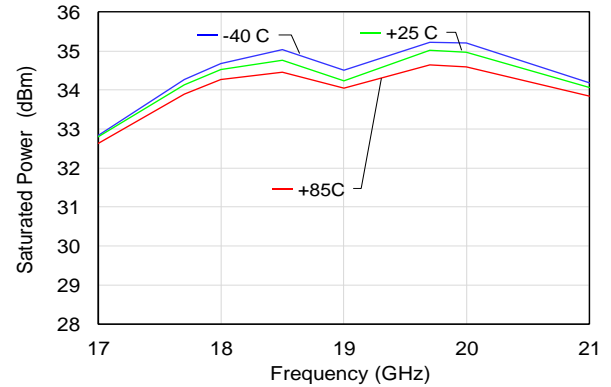
Output TOI vs. Frequency vs. Temperature



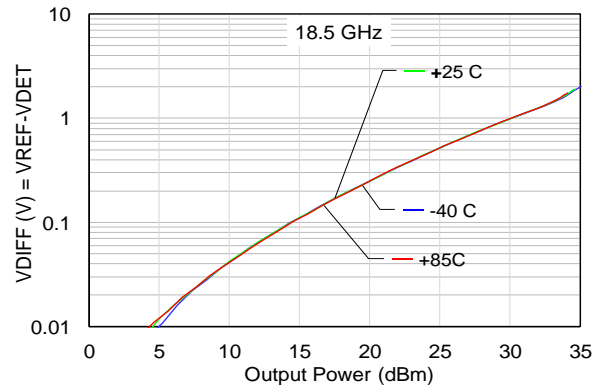
P1dB vs. Frequency vs. Temperature



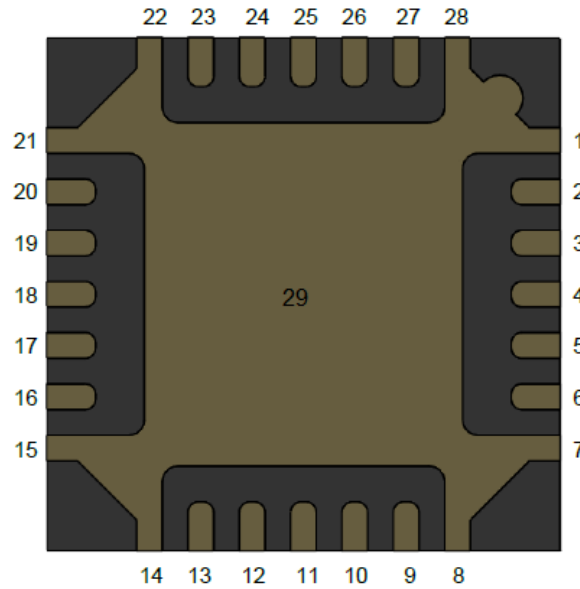
Saturated Power vs. Frequency vs. Temperature



Power Detector vs. Output Power vs. Temperature



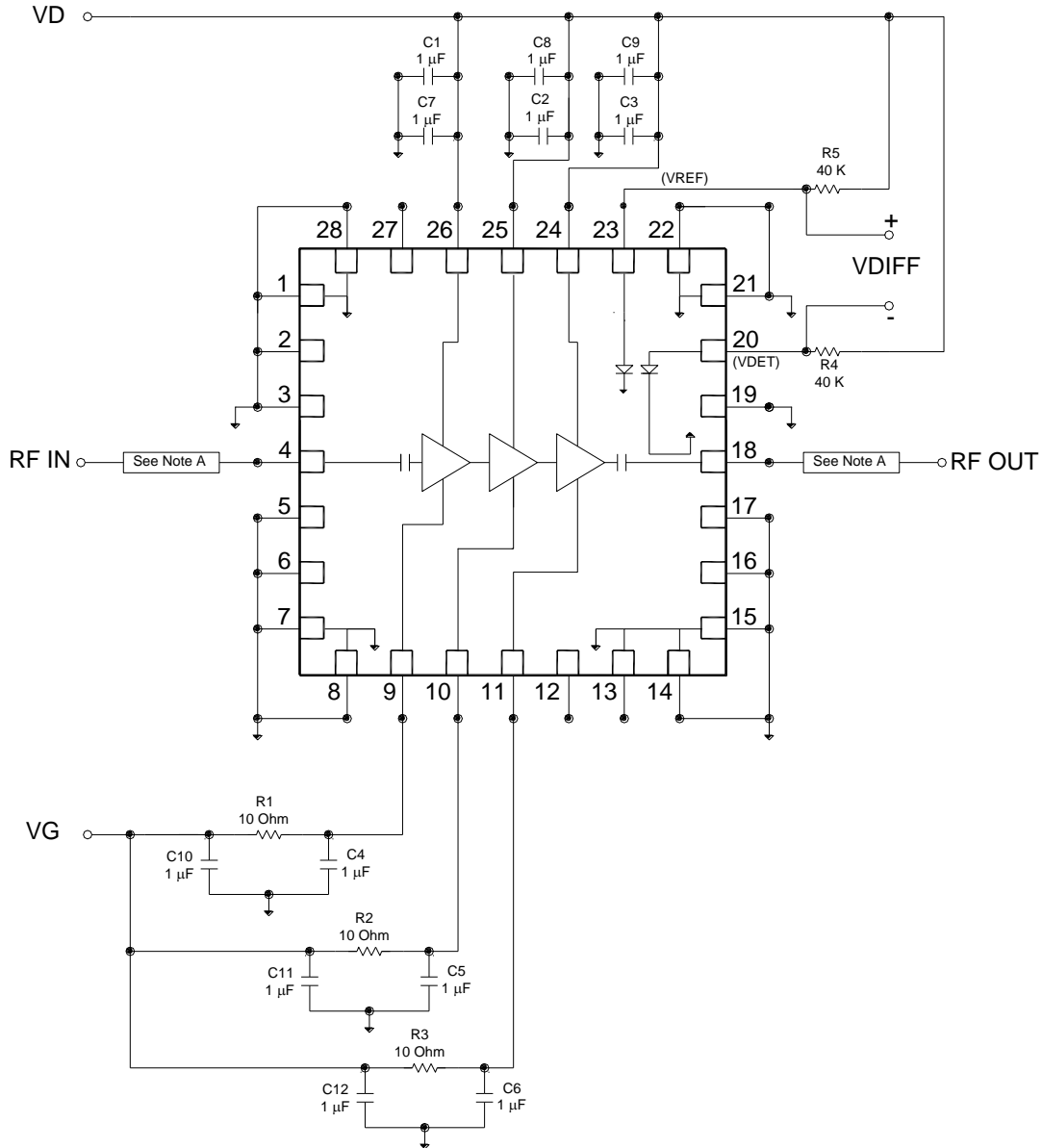
Pin Configuration and Description



Pin No.	Label	Description
1,7,8,14,15,21,22,28,29	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see 'PCB Mounting Pattern' on page 10 for suggested footprint
2,3,5,6,16,17,19	N/C	No internal connection; Recommend grounding these pins for best RF performance. See 'PCB Mounting Pattern' on page 10 for suggested footprint
4	RF IN	RF input, matched to 50 ohms
9	VG1	Stage 1 gate voltage ⁽¹⁾
10	VG2	Stage 2 gate voltage ⁽¹⁾
11	VG3	Stage 3 gate voltage ⁽¹⁾
12, 27	N/C	No internal connection; May be grounded on PCB or left open
13	GND	Internally connected to GND. May be grounded on the PCB or left open
18	RF OUT	RF output, matched to 50 ohms
20	VDET	Detector diode output voltage. Varies with RF output power
23	VREF	Reference diode output voltage
24	VD3	Stage 3 drain voltage ⁽¹⁾
25	VD2	Stage 2 drain voltage ⁽¹⁾
26	VD1	Stage 1 drain voltage ⁽¹⁾

(1) Bias bypass network is required; see 'Application Circuit' on page 8 as an example

Applications Circuit



Note A: 50 Ω Microstrip Transmission Line.

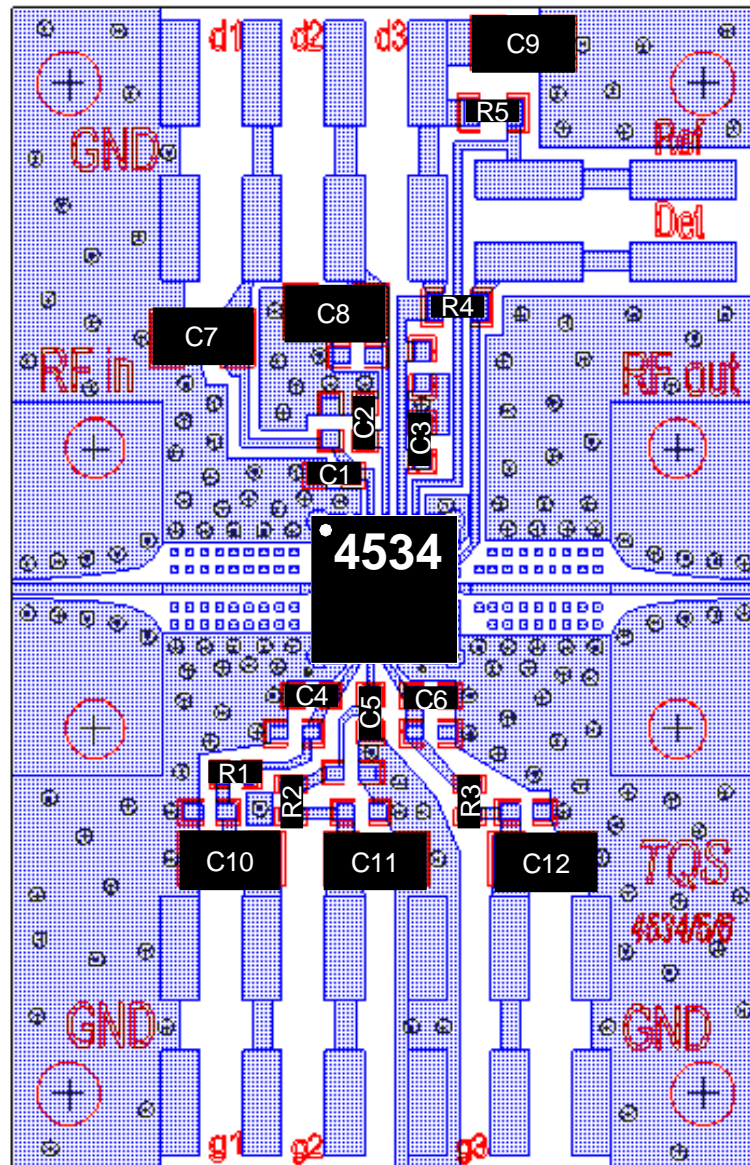
Bias Up Procedure

1. Set I_D limit to 2800 mA, I_G limit to 60 mA
2. Set V_G to -1.5 V
3. Set V_D +6 V
4. Adjust V_G more positive until $I_{DQ} = 1430$ mA
($V_G \sim -0.4$ V to -0.8 V typical range)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Reduce V_G to -1.5 V. Ensure $I_{DQ} \sim 0$ mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board Layout

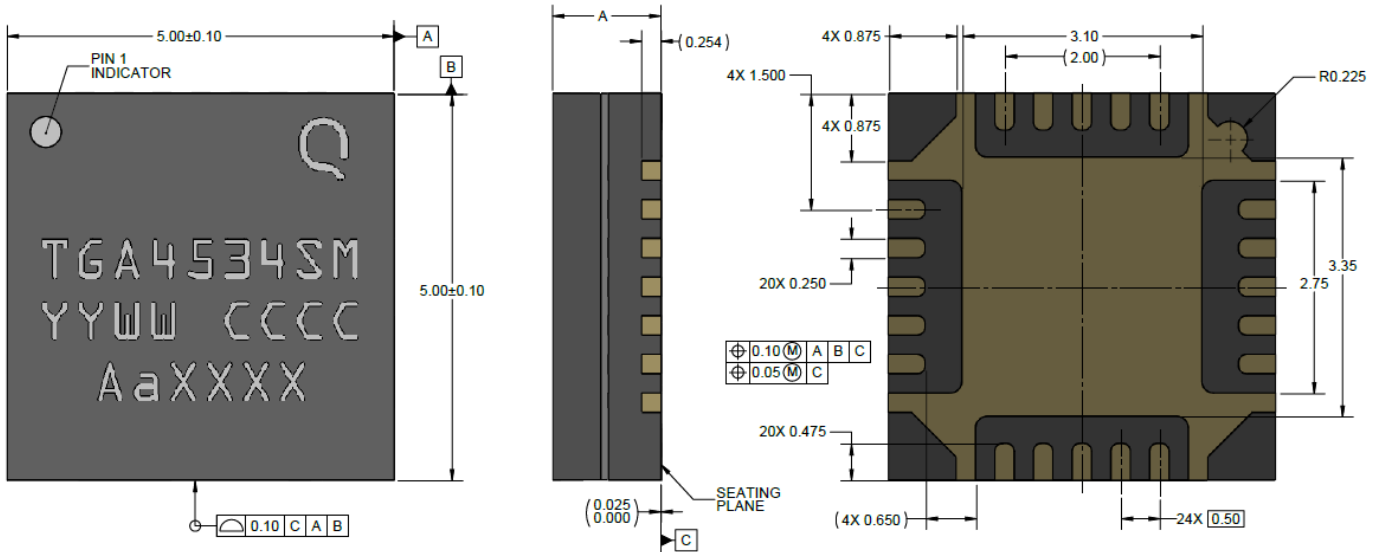


Board material is Rogers Corp. 4003 0.008" thickness with ½ oz copper cladding.
For further technical information, refer to the [TGA4534-SM](#) Product Information page.

Bill of Material

Ref. Des.	Value	Description	Manuf.	Part Number
U1		K Band Power Amplifier	Qorvo	TGA4534-SM
C1 thru C6	1.0 µF	Cap, 0402, 25 V, 10%, X5R SMD	Various	
C7 thru C12	1.0 µF	Cap, 0805, 25 V, 10%, X5R SMD	Various	
R1, R2, R3	10 Ω	Res, 0402, 0.06 W, 5%, SMD	Various	
R4, R5	40 kΩ	Res, 0402, 0.06 W, 5%, SMD	Various	

Package Marking & Dimensions



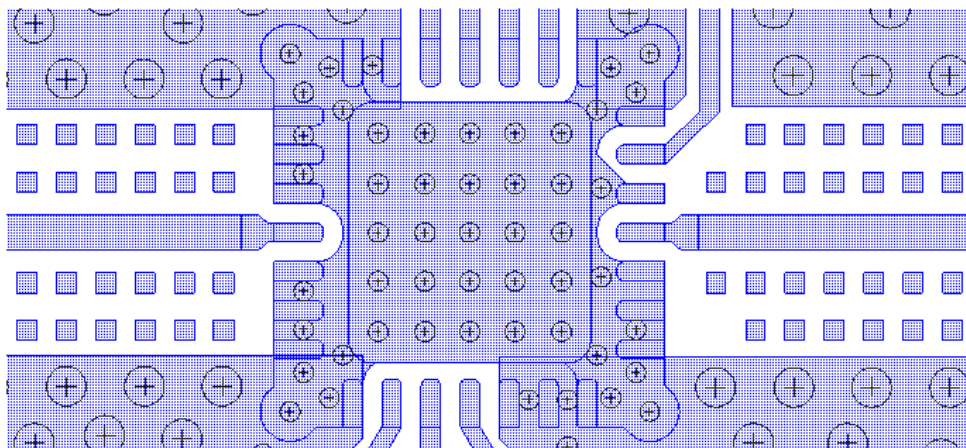
LASER MARK NOTES:

- YY IS THE LAST TWO DIGITS OF THE CALENDAR YEAR AND WW IS THE WEEK NUMBER OF THE ASSEMBLY LOT START.
- CCCC IS COUNTRY CODE.
- Aa IS VENDOR (AC).
- XXXX IS THE BATCH ID.

A	ACSLP
MAX.	1.400
NOM.	1.300
MIN.	1.200

NOTES: UNLESS OTHERWISE SPECIFIED;
1. PACKAGE LEADS ARE GOLD PLATED.

PCB Mounting Pattern



Notes:

1. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias have a final plated thru diameter of .25 mm (.010").

Thermal and Reliability Information

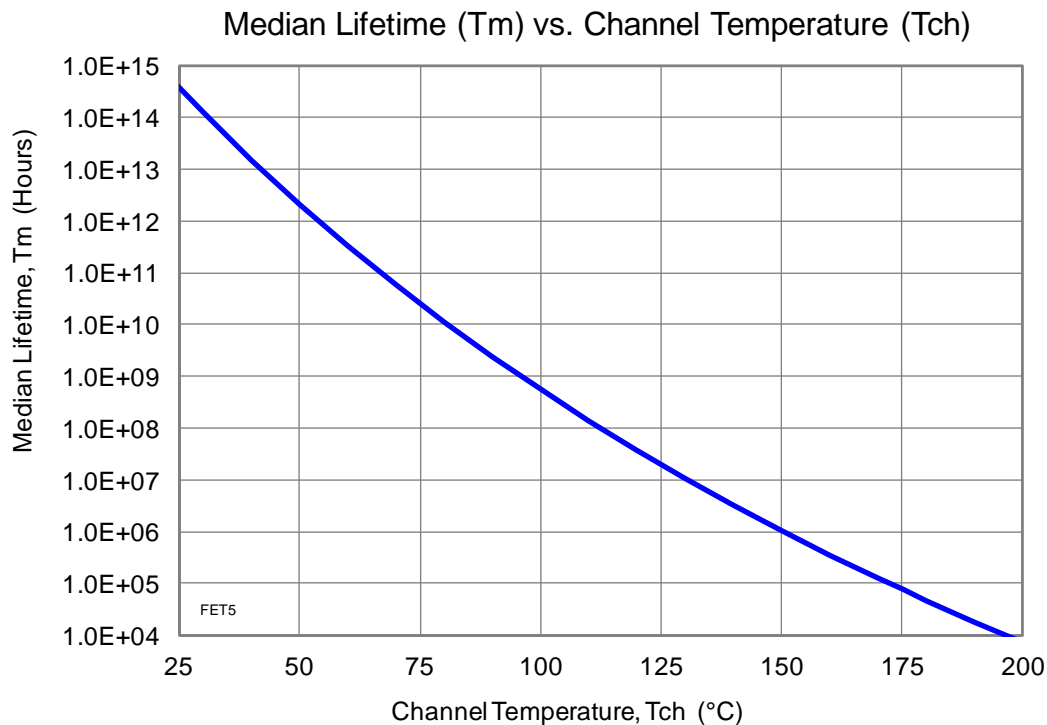
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{base} = 85^{\circ}C$, $V_D = 6 V$, $I_{DQ} = 1430 mA$ $P_{DISS} = 8.6 W$	5.75	$^{\circ}C/W$
Channel Temperature (T_{CH}) (No RF Drive)		134	$^{\circ}C$
Median Lifetime (T_M)		6.6E+6	Hrs
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{base} = 85^{\circ}C$ $V_D = 6 V$, $I_{DD} = 2100 mA$ $P_{OUT} = 34.2 dBm$, $P_{DISS} = 10 W$	5.75	$^{\circ}C/W$
Channel Temperature (T_{CH}) (Under RF Drive)		143	$^{\circ}C$
Median Lifetime (T_M)		2.4E+6	Hrs

Notes:

1. Thermal resistance is measured to back of the package.

Median Lifetime

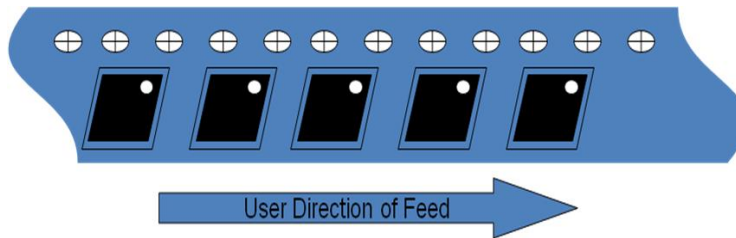
Test Conditions: $V_D = 6 V$
 Failure Criteria = 10% reduction in I_{D_MAX}



Tape and reel Information

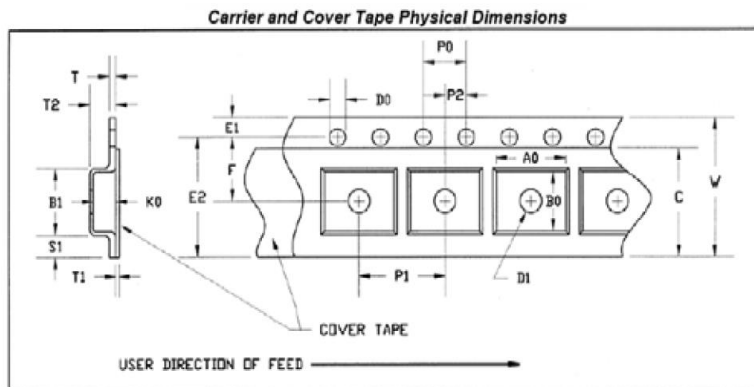
Standard T/R size = 500 pieces on a 7" reel

Vendor: Tek-Pak P/N QFN0500x0500F-L500



CARRIER AND COVER TAPE DIMENSIONS

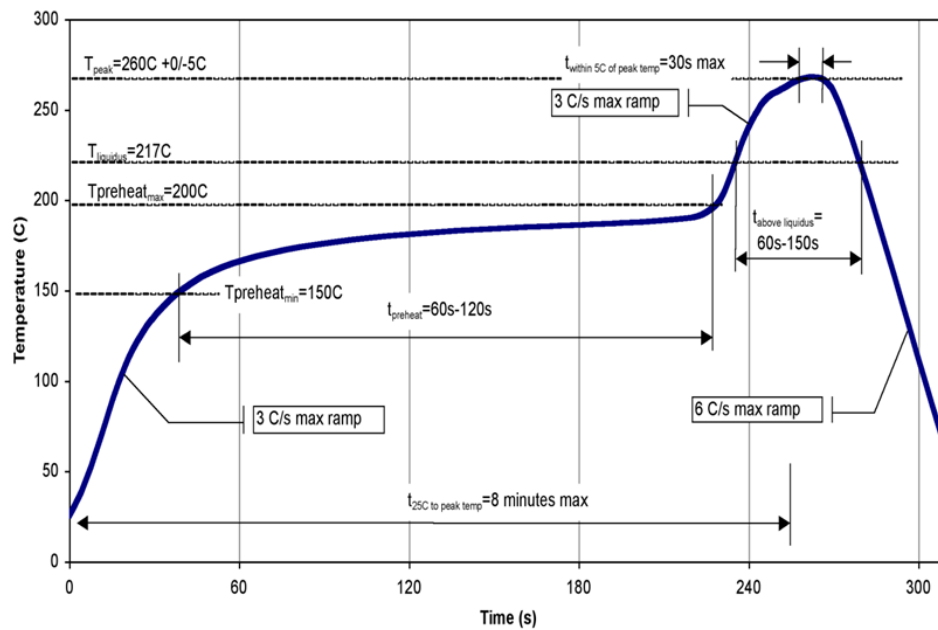
Part	Feature	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.3
	Width	B0	0.209	5.3
	Depth	K0	0.064	1.65
	Pitch	P1	0.315	8.00
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12.00



Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C
2. The use of no-clean solder to avoid washing after soldering is recommended.
3. Do not expose the package lid to temperatures > 280 °C

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 0	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free
- Qorvo Green



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: [1-844-890-8163](tel:1-844-890-8163)

Web: www.qorvo.com

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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