



TQP3M9036

Ultra Low-Noise, High Linearity LNA

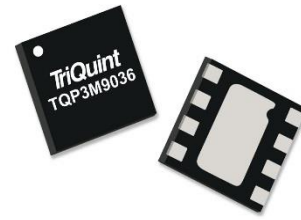
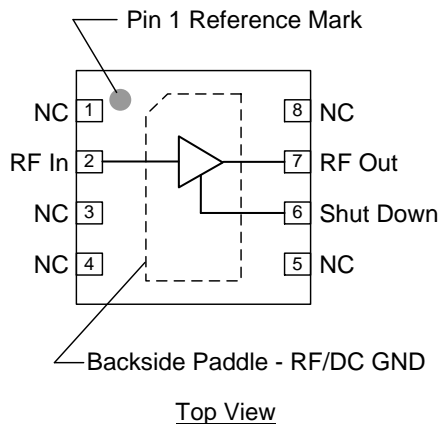
Product Overview

The TQP3M9036 is a high linearity, ultra low noise gain block amplifier in a small 2x2 mm surface-mount package. At 900 MHz, the amplifier typically provides high 19.8 dB gain, +36 dBm OIP3, and 0.45 dB Noise Figure while drawing 68 mA current from a 5V supply. The amplifier does not require any negative supplies for operation and can be biased from positive supply rails from 3.3 to 5 V. The device is housed in a lead-free/green/RoHS-compliant industry-standard 2x2 mm package.

The TQP3M9036 is internally matched using a high performance E-pHEMT process and only requires 4 external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. The low noise amplifier contains an internal active bias to maintain high performance over temperature and integrates a shut-down biasing capability for TDD applications.

The TQP3M9036 covers the 100–2000 MHz frequency band and is targeted for wireless infrastructure. The LNA is pin compatible with the high-band, 1500–2700 MHz TQP3M9037.

Functional Block Diagram



8-pin 2x2 mm DFN Package

Key Features

- 100–2000 MHz Operational Bandwidth
- Ultra low noise figure, 0.45 dB NF at 900 MHz
- High gain, 19.8 dB Gain at 900 MHz
- High linearity, +36 dBm Output IP3
- High input power ruggedness, >22 dBm $P_{IN, MAX}$
- Unconditionally stable
- Integrated on-chip matching, 50 ohm in/out
- Integrated active bias
- Integrated shutdown control pin
- 3-5 V positive supply voltage: $-V_{gg}$ not required
- Pin compatible with high-band TQP3M9037

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
TQP3M9036	Ultra low noise, High IP3 LNA
TQP3M9036-PCB	100–2000 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 7" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power, CW, 50 Ω, T=+25 °C	+22 dBm
Device Voltage (V _{DD})	+7 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V _{CC})	+3.3	+5.0	+5.25	V
T _{CASE}	-40		+105	°C
T _j for >10 ⁶ hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5V, Temp=+25°C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		100		2000	MHz
Test Frequency			900		MHz
Gain		18.2	19.8	21.2	dB
Input Return Loss	Note 1		13		dB
Output Return Loss	Note 1		11		dB
Output P1dB			+20		dBm
Output IP3	P _{out} =+5 dBm/tone, Δf=1 MHz	+32	+36		dBm
Noise Figure			0.45	0.75	dB
Power Shutdown Control ⁽³⁾	On state	0		0.4	V
	Off state (Power down)	2.5	3.3	V _{DD}	V
Current, I _{DD}	On state	40	68	90	mA
	Off state (Power down)		3	4	mA
Shutdown pin current, I _{SD}	V _{PD} ≥ 3 V		140		μA
Switching Speed ⁽⁴⁾	ON time (50%Ctrl to 90% RF)		1		μs
	OFF time (50%Ctrl to 10% RF)		0.5		μs
Thermal Resistance, θ _{jc}	channel to case		62		°C/W

Notes:

1. Input and output return loss can be improved to better than 15 dB with minimal impact on noise figure by adjusting the values of the bias inductor and output DC blocking capacitor. Refer to the Optimized Return Loss reference design on page 7.
2. Current can be reduced by operating at a lower device voltage. (example: I_{dd}=50 mA at V_{dd}=4 V)
3. Voltage referred to J5 turret on evaluation board (pg.4).
4. Switching speed can be improved by reducing the value of C1 of schematic on pg. 4.

Pin 6 (V_{PD}) voltage limits

	min	Max	Units
V _{low}	0	0.1	V
V _{high}	0.5	V _{DD}	V

Device Characterization Data

S-Parameters

Test conditions unless otherwise noted: $V_{DD}=+5\text{ V}$, $I_{DD}=68\text{ mA}$ (typ.), $\text{Temp}=+25^{\circ}\text{C}$, 50 Ohm system

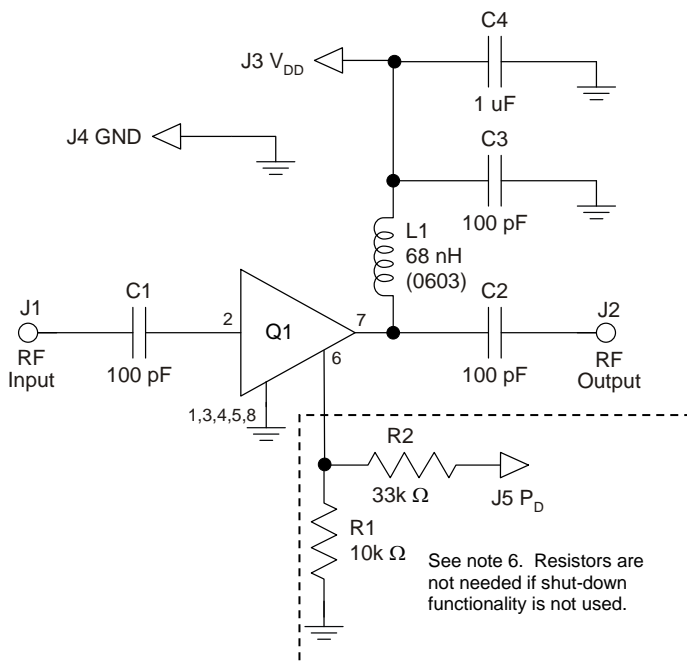
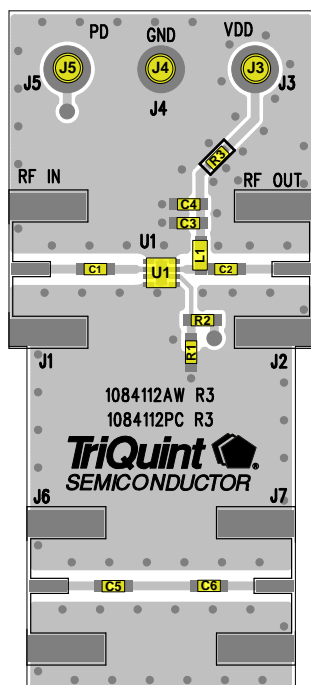
Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-7.1	-11.1	28.4	167.9	-33.8	13.3	-22.8	-2.8
100	-7.3	-13.5	28.1	160.6	-33.5	16.7	-20.1	27.8
200	-8.0	-20.6	27.2	145.9	-32.6	28.7	-15.8	32.8
400	-9.8	-30.6	24.8	124.1	-30.1	45.5	-12.4	17.7
600	-11.4	-34.6	22.5	109.8	-27.5	53.1	-11.3	4.5
800	-12.6	-36.2	20.6	99.5	-25.4	56.2	-10.9	-5.8
1000	-13.6	-36.1	19.0	91.3	-23.7	56.8	-10.6	-14.5
1200	-14.4	-35.7	17.6	84.4	-22.2	56.4	-10.5	-22.1
1400	-14.9	-34.8	16.4	78.3	-20.9	55.1	-10.4	-29.2
1600	-15.4	-33.9	15.4	72.7	-19.9	53.4	-10.3	-35.6
1800	-15.7	-33.2	14.4	67.6	-18.9	51.4	-10.2	-41.6
2000	-15.9	-32.6	13.6	62.8	-18.0	49.3	-10.2	-47.2
2200	-16.2	-32.1	12.8	58.2	-17.2	47.0	-10.2	-52.9
2400	-16.4	-31.3	12.1	53.8	-16.4	44.6	-10.2	-58.3
2600	-16.7	-30.5	11.5	49.5	-15.8	42.0	-10.2	-63.6
2800	-16.9	-29.6	10.9	45.3	-15.1	39.4	-10.3	-69.2

Noise Parameters

Test conditions unless otherwise noted: $V_{DD}=+5\text{ V}$, $I_{DD}=68\text{ mA}$ (typ.), $\text{Temp}=+25^{\circ}\text{C}$, 50 Ohm system

Freq (MHz)	NF _{min} (dB)	MagOpt (mag)	AngOpt (deg)	Rn (Ω)
700	0.356	0.187	10.9	0.062
900	0.452	0.174	22.2	0.060
1100	0.415	0.140	12.1	0.061
1300	0.406	0.142	23.7	0.062
1500	0.377	0.116	-6.64	0.069
1700	0.346	0.115	23.6	0.062

Application Circuit – TQP3M9036-PCB



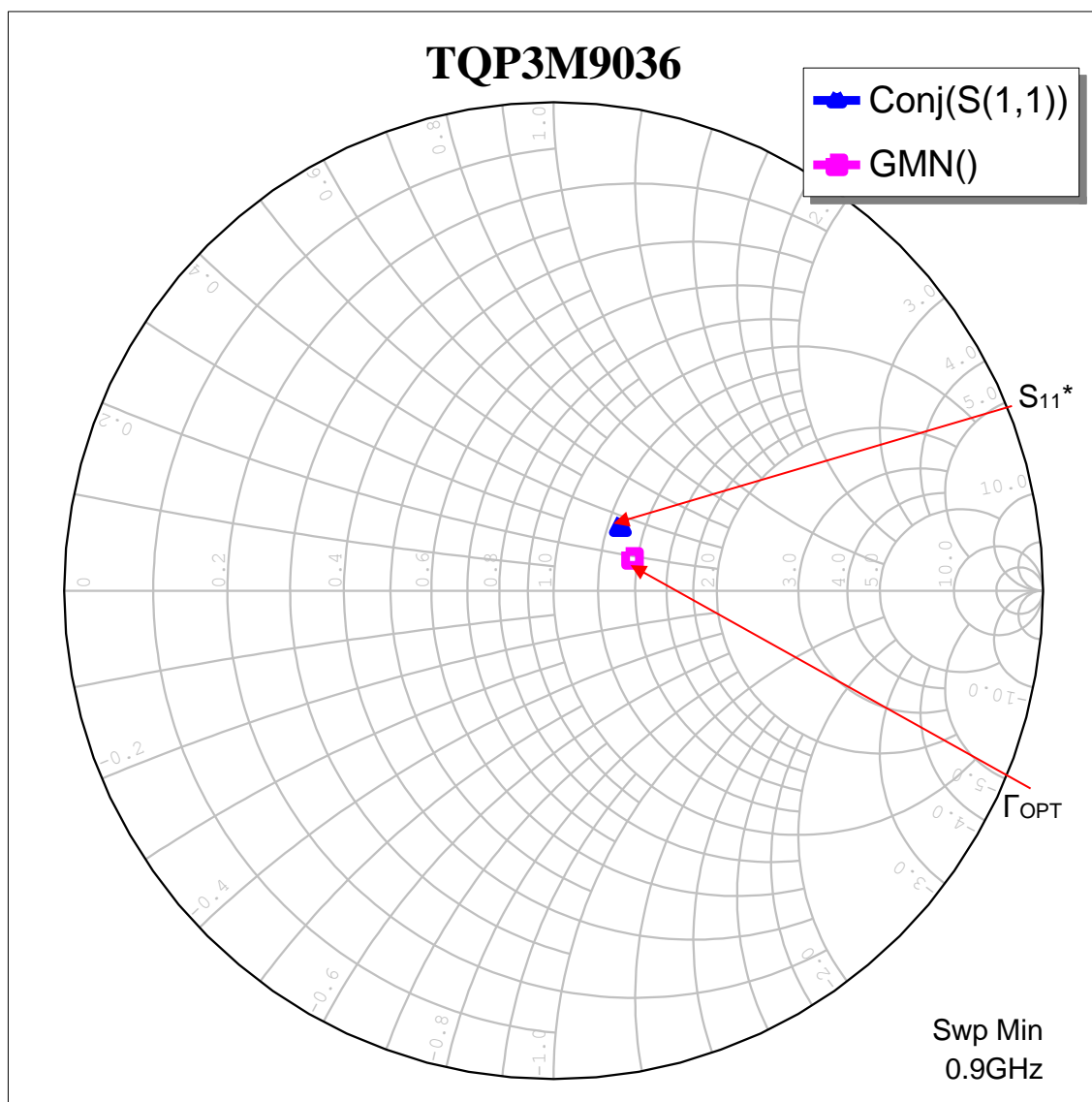
Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. C1, C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
5. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
6. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R1 and R2 are not loaded, the LNA will operate in its standard "ON" state.
7. A through line is included on the evaluation board for board loss measurement and de-embedding.

Bill of Material – TQP3M9036-PCB

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	TriQuint	1084112
U1	n/a	Ultra Low Noise, High Linearity LNA	TriQuint	TQP3M9036
R1	10K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R2	33K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
L1	68 nH	Inductor, 0603, 5%, Ceramic	various	various
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	various
C1, C2, C3, C5, C6	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	various
J3, J4, J5	n/a	Solder Turret	various	various

Γ_{opt} and S_{11}^*



Typical Performance – TQP3M9036-PCB VDD = 5 V, 25°C

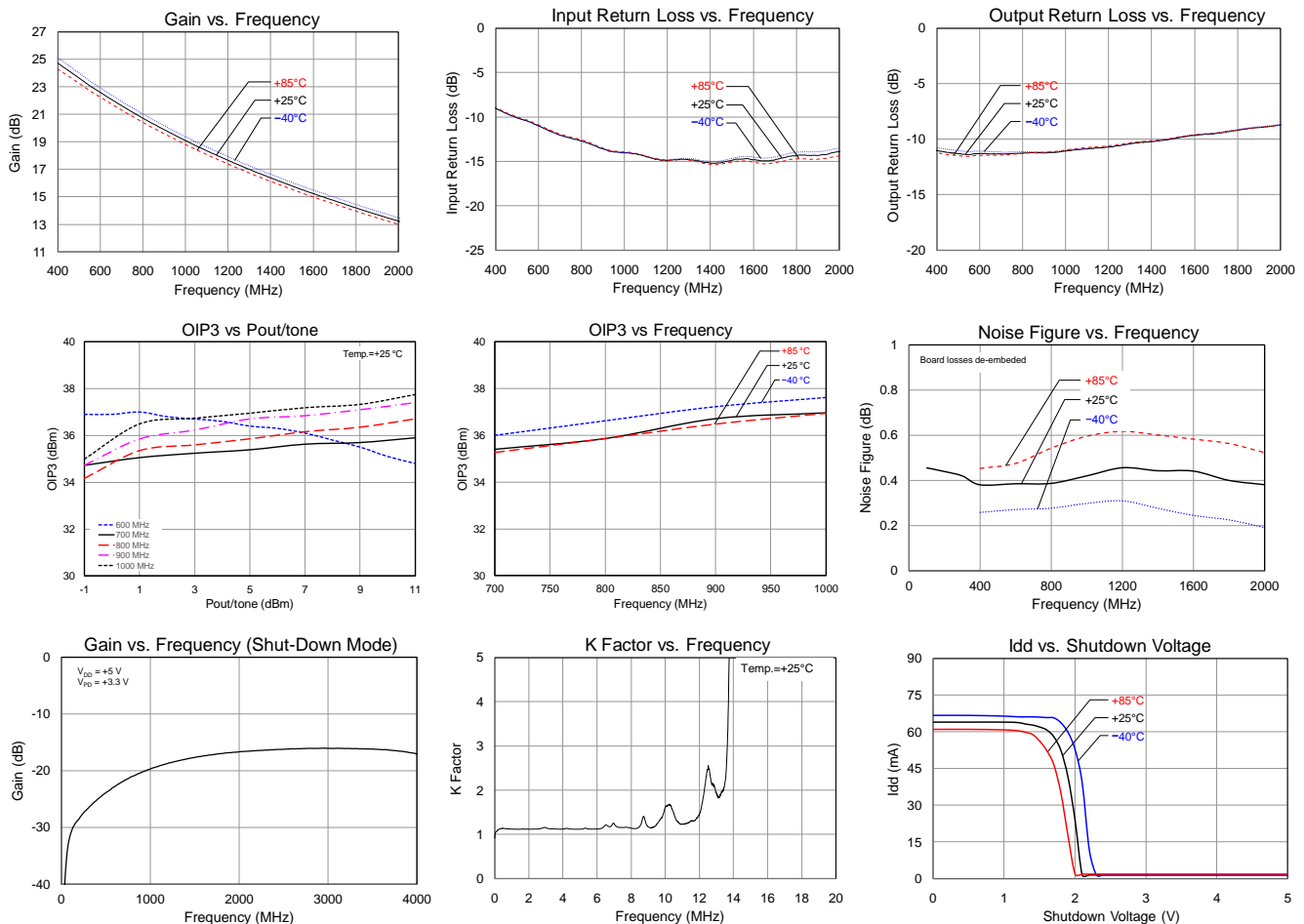
Parameter	Conditions	Typical Value					Units
Frequency		600	700	900	1500	2000	MHz
Gain		22.5	20.8	19.1	15.1	13	dB
Input Return Loss		-11	-11.2	-12.7	-14.3	-13.5	dB
Output Return Loss		-11.5	-10.4	-11.0	-11.1	-8.6	dB
Output P1dB		+23.5	+23.1	+23.2	+23.2	+23.2	dBm
Output IP3	Pout= +5 dBm/tone, $\Delta f=1$ MHz	+36	+34.2	+35.2	+36	+37	dBm
Noise figure ⁽¹⁾		0.38	0.38	0.4	0.44	0.52	dB

Notes:

1. Noise figure data shown in the table above is de-embedded from the eval board loss.

Performance Plots – TQP3M9036-PCB VDD = 5 V

Test conditions unless otherwise noted: VDD = +5 V, IDD = 68 mA, T_{CASE} = +25°C, 50 Ω system



Typical Performance – TQP3M9036-PCB VDD = 3.3 V

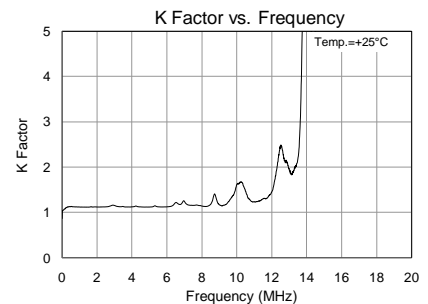
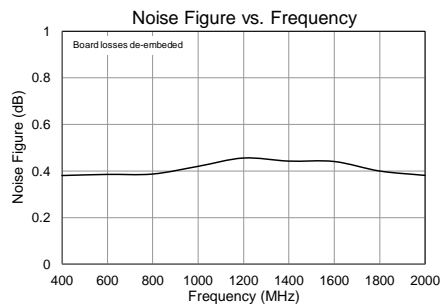
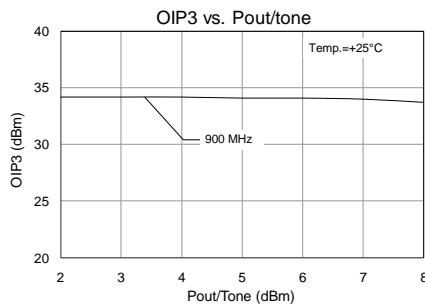
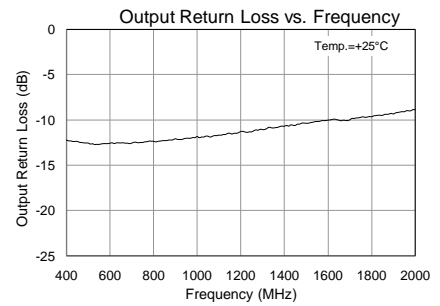
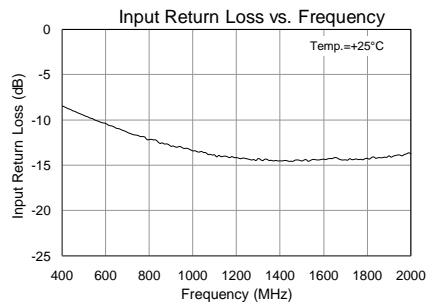
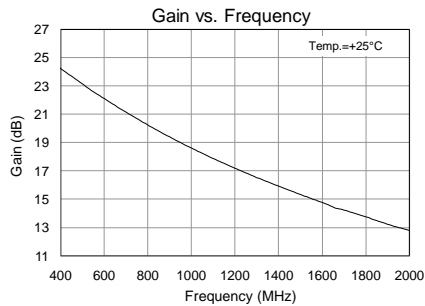
Parameter	Conditions	Typical Value				Units
Frequency		700	900	1500	2000	MHz
Gain		21	19.3	15.3	12.8	dB
Input Return Loss		10.6	12.2	14.3	13.8	dB
Output Return Loss		11.8	11.5	10	8.7	dB
Output P1dB		+17.7	+18.1	+20.5	+20.7	dBm
Output IP3	Pout= +5 dBm/tone, $\Delta f=1$ MHz	+31.1	+31.7	+32.9	+33.7	dBm
Noise figure ⁽¹⁾		0.38	0.4	0.44	0.52	dB

Notes:

- Noise figure data shown in the table above is de-embedded from the eval board loss.

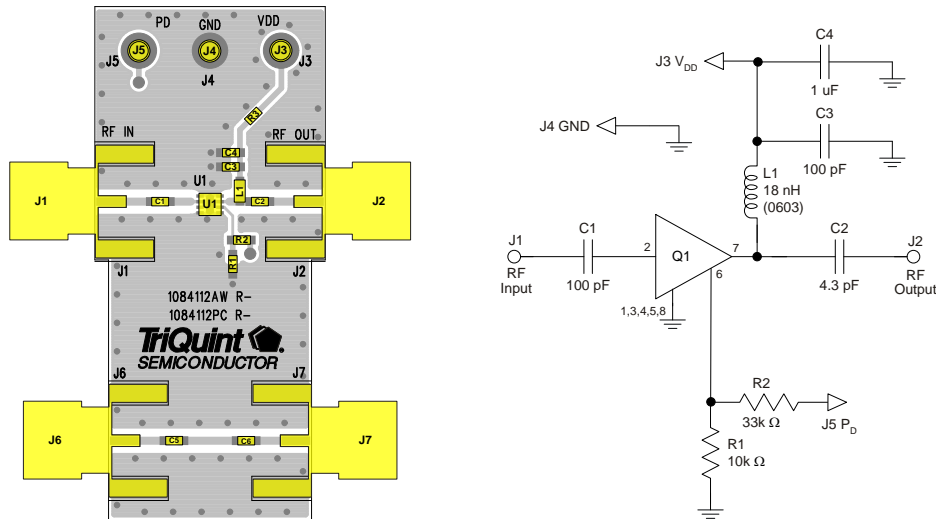
Performance Plots – TQP3M9036-PCB VDD = 3.3 V

Test conditions unless otherwise noted: V_{DD} = +3.3 V, I_{DD} = 45 mA, T_{CASE} = +25°C, 50 Ω system



Reference Design – 690-920 MHz Optimized Return Loss

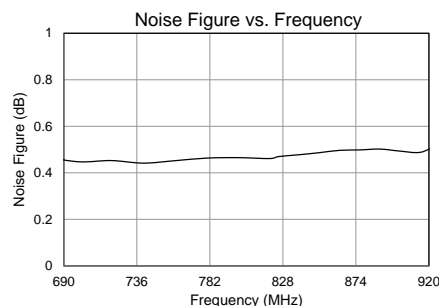
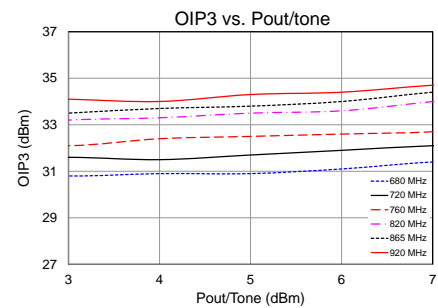
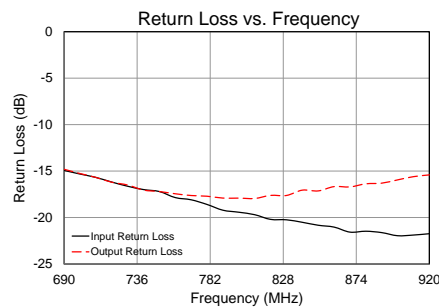
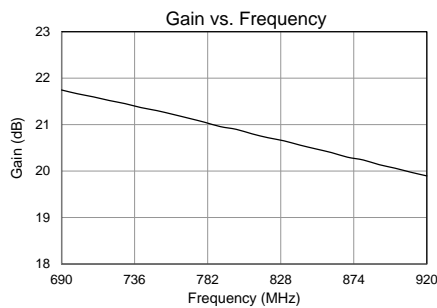
The following reference design provides improved input/output return loss in the 690-920 MHz band. This covers the low frequency UL bands.



Bill of Material

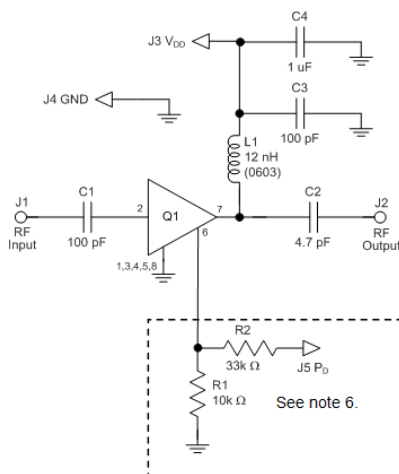
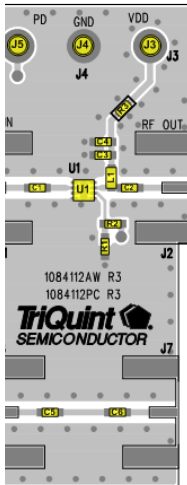
Reference Des.	Value	Description	Manuf.	Part Number
L1	18 nH	IND, 0603, 5%,	Coilcraft	0603HP-18NXJL
C1, C3, C5, C6	100 pF	CAP, 0402, 5%, 50V, NPO/COG	various	
C2	4.3 pF	CAP, 0402, ± 0.1 pF, 25V, ACCU-P	AVX	04023J4R3BBSTR
C4	1.0 uF	CAP, 0402, 10%, 10V, NPO, X5R	various	
R1	10K Ω	RES, 0402, 5%, 1/16W	various	
R2	33K Ω	RES, 0402, 5%, 1/16W	various	
R3	0 Ω	RES, 0402, 5%, 1/16W	various	

RF Performance Plots



Reference Design – 860-960 MHz Optimized Return Loss

The following reference design provides improved output return loss in the 860-960 MHz band. This is achieved via adjustment of the values of the existing bias inductor and output DC blocking capacitor.



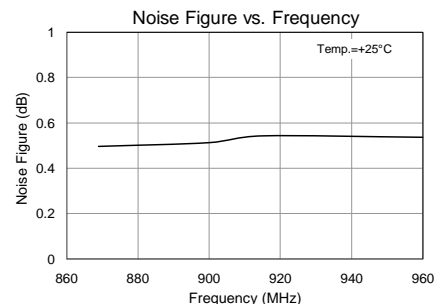
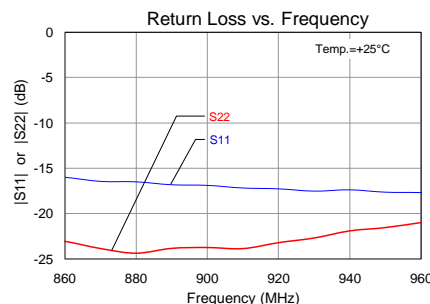
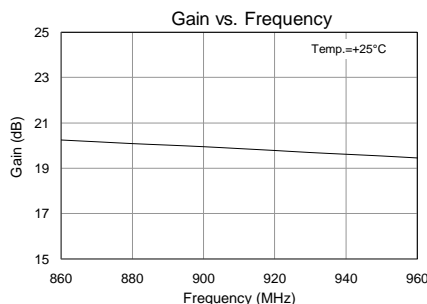
Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. Distance from the right edge of U1 to the left edge of C2 is 115 mils.
5. C1 and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
6. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications.
7. If R1 and R2 are not loaded, the LNA will operate in its standard "ON" state.
8. A through line is included on the evaluation board for board loss measurement and de-embedding.

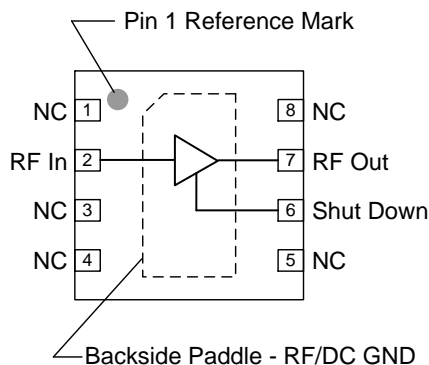
Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	TriQuint	
U1	n/a	TQP3M9036 Sample	TriQuint	TQP3M9036
L1	12 nH	IND, 0603, 5%, CHIP	various	
C1, C3, C5, C6	100 pF	CAP, 0402, 5%, 50V, NPO/COG	various	
C2	4.7 pF	CAP, 0402, ± 0.1 pF, 50V, U-Series	AVX	04025U4R7BAT2A
C4	1.0 uF	CAP, 0402, 10%, 10V, NPO, X5R	various	
R1	10K Ω	RES, 0402, 5%, 1/16W	various	
R2	33K Ω	RES, 0402, 5%, 1/16W	various	
R3	0 Ω	RES, 0402, 5%, 1/16W	various	

RF Performance Plots



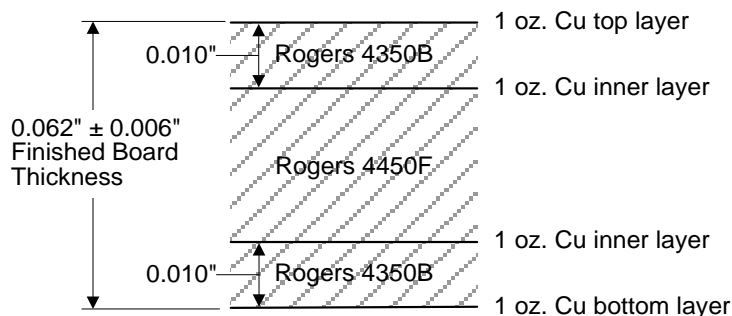
Pin Configuration and Description



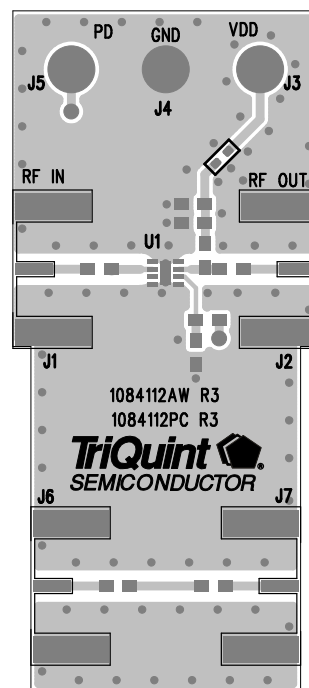
Pin No.	Label	Description
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage turns off the device. If the pin is not connected or is less than 1V, then the device will operate under its normal operating condition.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

TriQuint PCB 1084112 Material and Stack-up



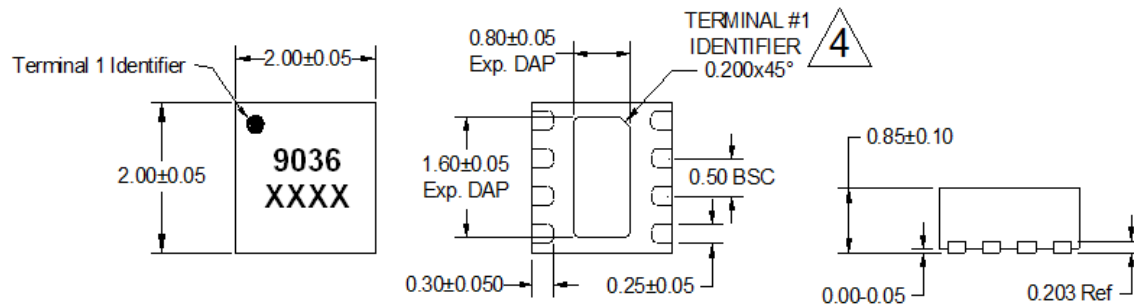
50 ohm line dimensions: width = .020", spacing = .032"



Mechanical Information

Package Marking and Dimensions

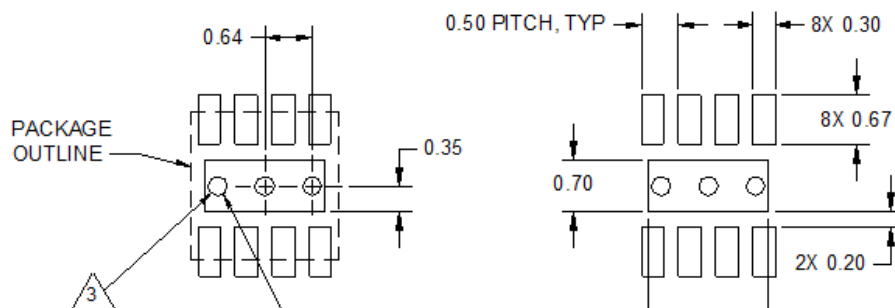
Marking: Part number – 9036
Lot Code – XXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35 mm ($\#80/.0135$ ") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10 ").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C2	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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