

RFFM6500

2.7V to 4.2V, 168MHz to 171MHz ISM Band
Transmit/Receive Module

The RFFM6500 is a single-chip front end module (FEM) for application in the 168MHz to 171MHz ISM Band. The RFFM6500 addresses the need for aggressive size reduction for typical portable equipment RF front end designs and greatly reduces the number of components outside of the core chipset thus minimizing the footprint and assembly cost of the overall solution. The RFFM6500 contains an integrated 1/2W PA, Tx/Rx SP2T RF switch, low pass filter, Si logic controller, and matching components. The RFFM6500 is packaged in a 32-pin, 6.0mm x 6.0mm x 1.2mm over-molded laminate package.



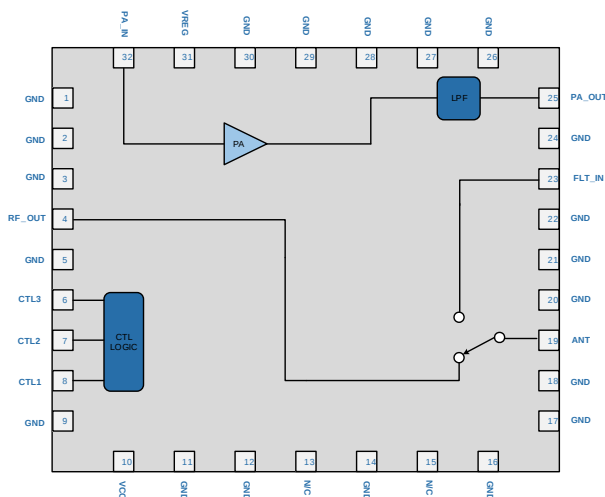
Package: LGA, 32-pin,
6.0mm x 6.0mm x 1.2mm

Features

- Tx Output Power: 27dBm
- Separate Rx/Tx 50Ω Transceiver Interface
- Low Pass Filter

Applications

- Wireless Automated Metering
- Wireless Alarm Systems
- Portable Battery Powered Equipment
- Smart Energy
- 168MHz/171MHz ISM Band Application
- Single Chip RF Front End Module



Functional Block Diagram

Ordering Information

RFFM6500SB	Standard 5-piece bag
RFFM6500SQ	Standard 25-piece bag
RFFM6500SR	Standard 100-piece reel
RFFM6500TR13	Standard 2500-piece reel
RFFM6500PCK-410	Fully assembled evaluation board w/ 5-piece bag

Absolute Maximum Ratings

Parameter	Rating	Unit
Voltage	5.25	V _{DC}
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range	-40 to +85	°C
Maximum Input Power to PA, pin 32 (no damage)	+5	dBm
Maximum Input Power to Antenna Port, pin 19	+10	dBm
Moisture Sensitivity Level	MSL3	



Caution! ESD sensitive device.



RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

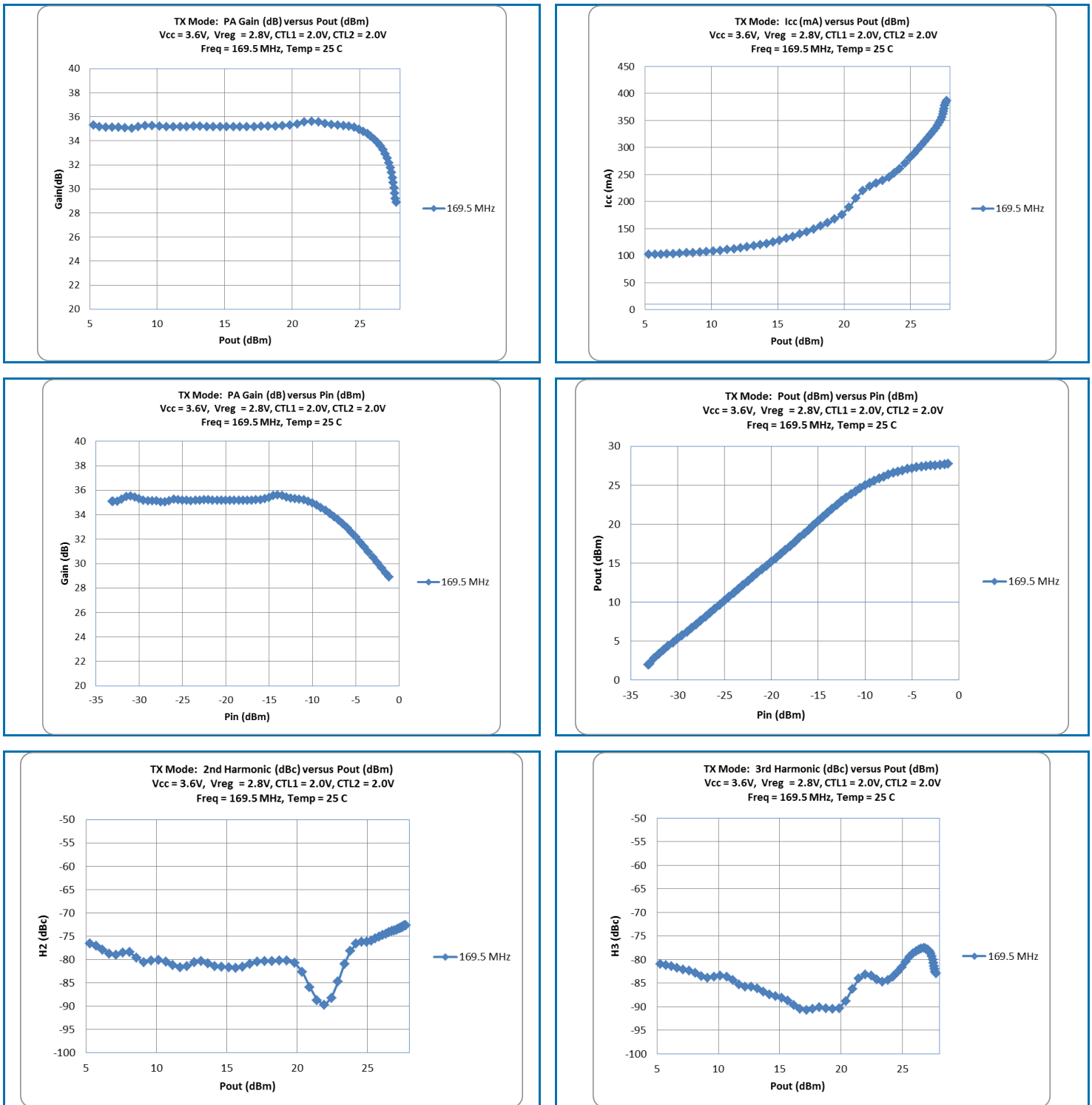
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Overall					
Active Frequency	168	169.5	171	MHz	
RF Port Impedance		50		Ω	
ESD, Human Body Model	500			V	RF Pins
ESD, Human Body Model	500			V	All Other Pins
ESD, Charge Device Model	500			V	RF Pins
ESD, Charge Device Model	500			V	All Other Pins
Leakage Current					V_{CC} = 3.6V, CTL1 = 2.8V, CTL2 = 2.8V, V_{REG} = 2.8V, Temperature = 25°C
I _{CC}		1	5	μA	
Transmit Mode					V_{CC} = 3.6V, CTL1 = CTL2 = V_{REG} = 2.8V, Temperature = 25°C
Power Supply Voltage	2.7	3.6	4.2	V	PA V _{CC}
Input Power		0	5	dBm	Pin 32
Output Power	25	27		dBm	Over all rated voltage and temperature conditions
Thermal Resistance		26.28		C°/W	4V V _{CC} , 100% Duty, 27dBm P _{OUT} , T _{REF} = 85° C
Operating Current		325	400	mA	P _{OUT} = 27dBm, V _{CC} = 3.6V, Temperature = 25°C
Large Signal Gain	27	30		dB	
Power Control Range	1.4		2.0	V	P _{OUT} = +7dBm to +27dBm (220nF capacitor to GND included on VREG pin)
	2.0		2.8	V	P _{OUT} = +24.0dBm to +27.5dBm
Module PAE (Power Added Efficiency)		43		%	V _{CC} = 3.6V, V _{REG} = 2.8V, P _{OUT} = 27dBm (takes into account filter and switches)
2nd Harmonic		-70	-67	dBc	
3rd to 10th Harmonic		-85	-72	dBc	
Input Return Loss			-10	dB	Measured at PA-IN Port at Pin 32
PA Turn-On Time		200		nS	Output stable to within 90% of final value
PA Turn-Off Time		200		nS	Output stable to within 90% of final value

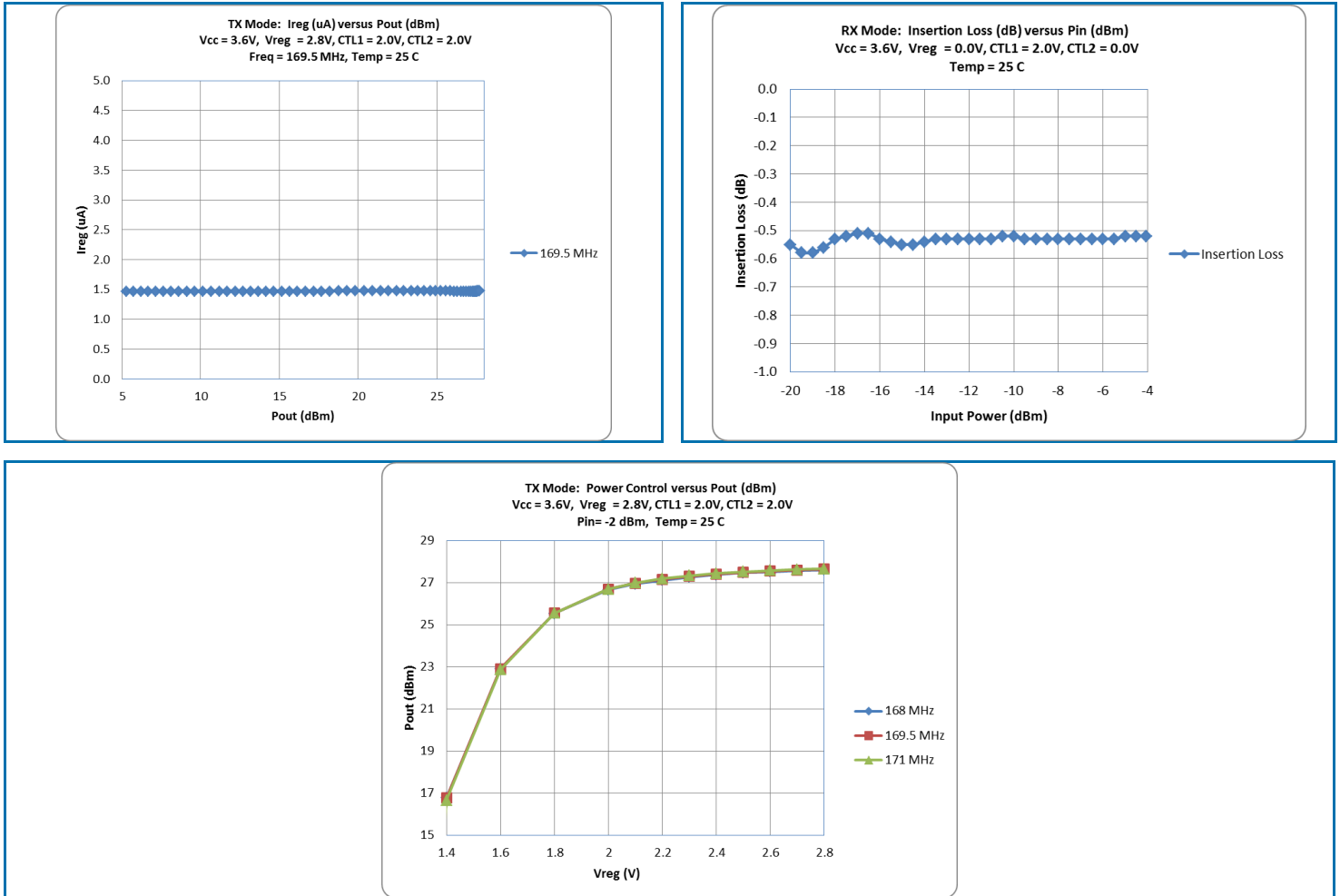
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Receive Mode					$V_{CC} = 3.6V$, $CTL1 = 2.8V$, $CTL2 = 0.0V$, $V_{REG} = 0.0V$, Temperature = 25°C
Insertion Loss		0.5	1.0	dB	
Input Return Loss		11		dB	
Output Return Loss		11		dB	
Power Supply Current		10	20	μA	$V_{CC} = 3.6V$, Temperature = 25°C
Antenna Switch Section					
Isolation	20			dB	From any used to unused port
Input Return Loss - Tx Mode		12	11	dB	
Input Return Loss - Rx Mode		14	11	dB	
Logic					
Control Current		0.25	1.0	μA	Control Voltage = 2.0V
I_{REG}		1.8	4.0	mA	Across all rated voltages at rated power

Switch Control Truth Table

Operating Mode	CTL1	CTL2	VREG	Typical Battery Current at $P_{OUT} = 27dBm$
Tx to ANT	1	1	2.8VDc	400mA
Rx from ANT	1	0	0VDc	10mA
Power Down	0	0	0VDc	50nA

Performance Plots

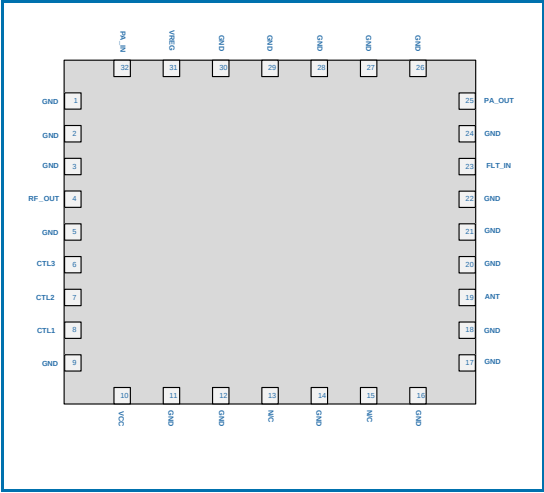




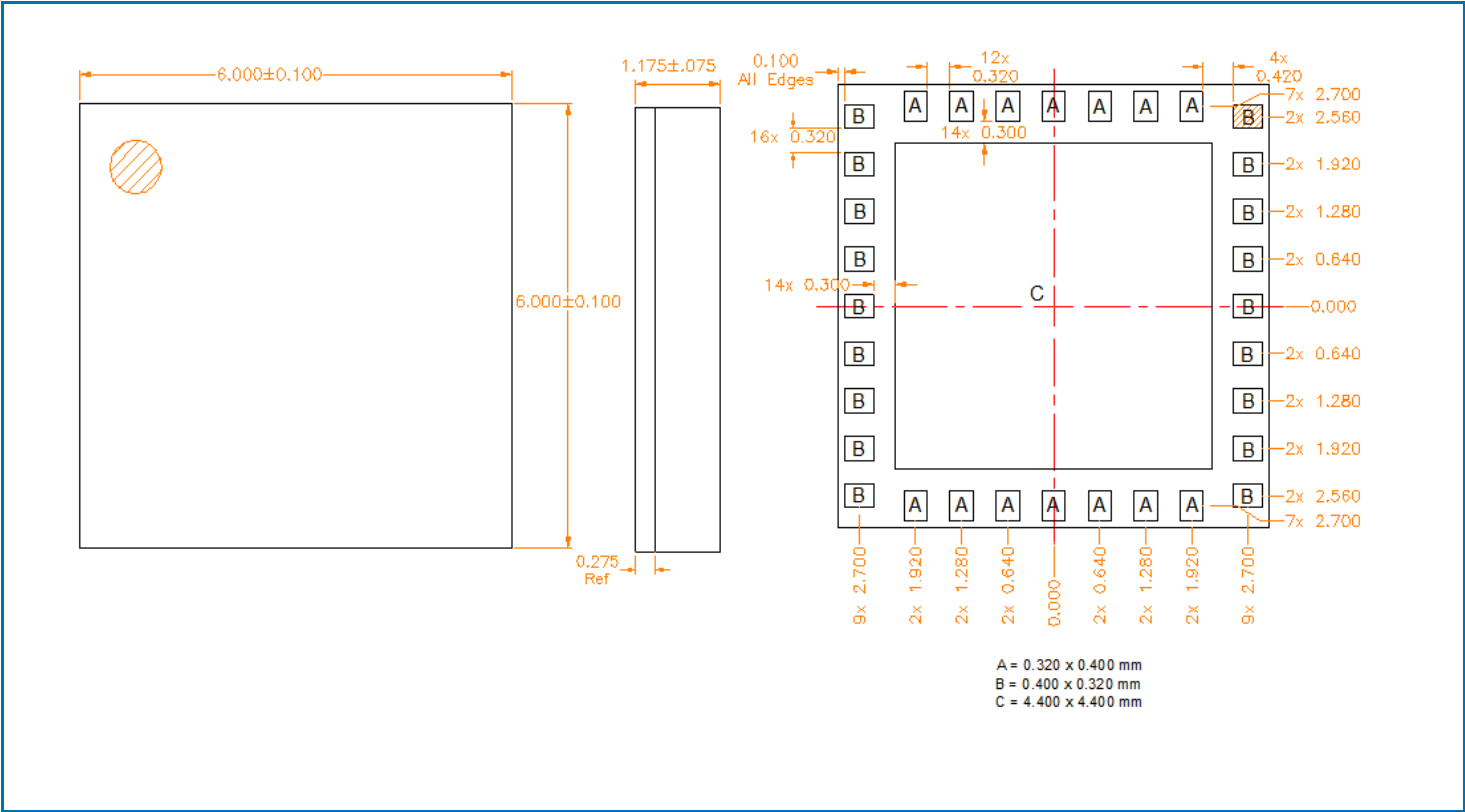
The schematic diagram illustrates the internal circuitry of the RFFM6500 module. The central component is the RFFM6500 IC, which is connected to various external components and connectors. The IC has pins numbered 1 through 32. Key connections include:

- Power and Ground:** Pin 1 is connected to ground. Pin 2 is connected to VREG. Pin 3 is connected to ground. Pin 4 is connected to VCC. Pin 5 is connected to ground. Pin 6 is connected to CTL2. Pin 7 is connected to ground. Pin 8 is connected to CTL1. Pin 9 is connected to ground. Pin 10 is connected to VCC. Pin 11 is connected to ground. Pin 12 is connected to ground. Pin 13 is connected to N/C. Pin 14 is connected to ground. Pin 15 is connected to N/C. Pin 16 is connected to ground. Pin 17 is connected to ground. Pin 18 is connected to ground. Pin 19 is connected to J3 ANT. Pin 20 is connected to ground. Pin 21 is connected to ground. Pin 22 is connected to ground. Pin 23 is connected to ground. Pin 24 is connected to ground. Pin 25 is connected to ground. Pin 26 is connected to ground. Pin 27 is connected to ground. Pin 28 is connected to ground. Pin 29 is connected to ground. Pin 30 is connected to ground. Pin 31 is connected to ground. Pin 32 is connected to J2 PA IN.
- Capacitors:** C3 (TBD) is connected between pins 10 and 11. C4 (TBD) is connected between pins 31 and 32. C5 (TBD) is connected between pins 23 and 24. C6 (TBD) is connected between pins 19 and 20.
- Inductors:** L1 (TBD) is connected between pins 25 and 26. L2 (THB) is connected between pins 23 and 24. L3 (TBD) is connected between pins 19 and 20. L6 (THB) is connected between pins 17 and 18.
- Connectors:** J1 (RX_OUT) is connected to pin 4. J2 (PA IN) is connected to pin 32. J3 (ANT) is connected to pin 19. P1 is a 6-pin connector with pins 1 through 6 connected to ground, VREG, VCC, CTL1, CTL2, and CTL2, respectively.

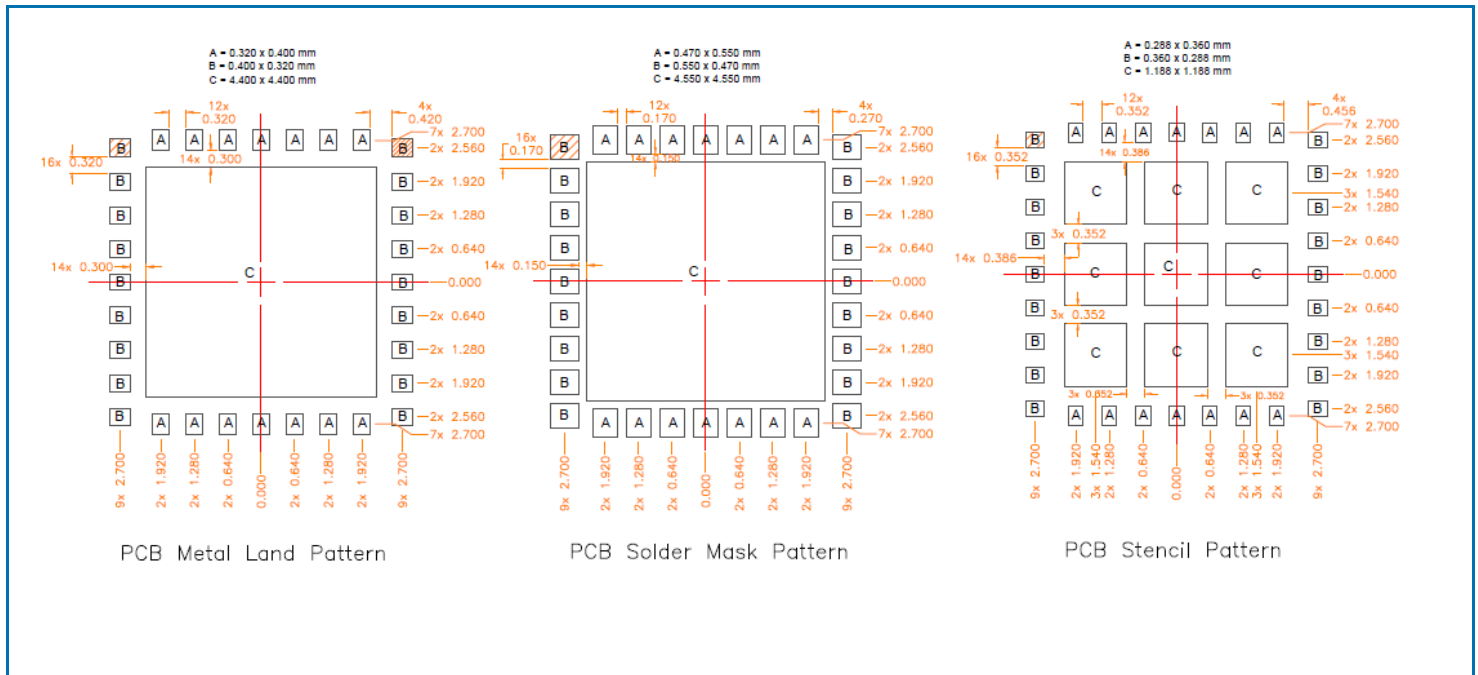
Pin Out



Package Drawing



PCB Patterns



Pin Names and Descriptions

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	RX_OUT	Receive Output Signal Port
5	GND	Ground
6	CTL3	Control logic for Si Controller, tied permanently to ground
7	CTL2	Control logic for Si Controller
8	CTL1	Control Logic for Si Controller
9	GND	Ground
10	VCC	Module Supply Voltage
11	GND	Ground
12	GND	Ground
13	N/C	Not connected in FEM. May be grounded on PCB if desired.
14	GND	Ground
15	N/C	Not connected in FEM. May be grounded on PCB if desired.
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	ANT	Antenna Output/Input
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	FLT_IN	Input to Low Pass Filter
24	GND	Ground
25	PA_OUT	Power Amplifier Output Signal Port
26	GND	Ground
27	GND	Ground
28	GND	Ground
29	GND	Ground
30	GND	Ground
31	VREG	Analog input voltage for Power Amplifier power control
32	PA_IN	Power Amplifier Input Signal Port