QPF4006

37 – 40.5 GHz GaN Front End Module

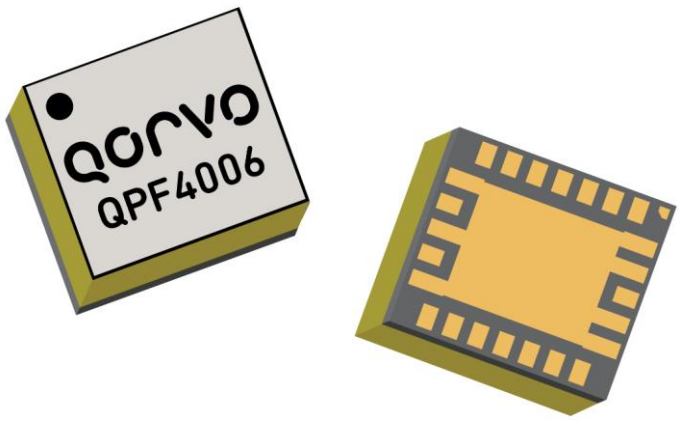
Product Description

The QPF4006 is a multi-function Gallium Nitride MMIC front-end module targeted for 39 GHz phased array 5G base stations and terminals. The device combines a low noise high linearity LNA, a low insertion-loss high-isolation TR switch, and a high-gain high-efficiency multi-stage PA.

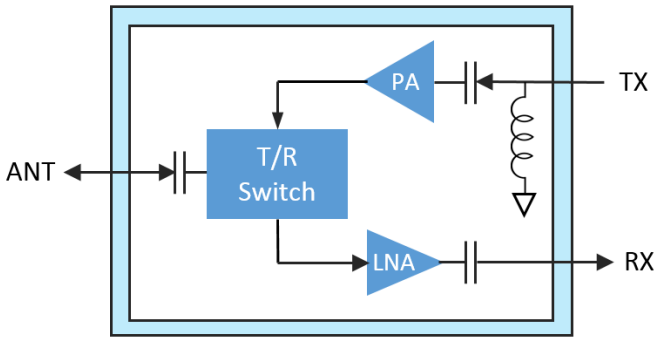
The QPF4006 operates from 37 GHz to 40.5 GHz range. The receive path (LNA+TR SW) is designed to provide 18dB of gain and a noise figure less than 4.5 dB. The transmit path (PA+SW) provides 23 dB of small signal gain and a saturated output power of 2 W.

The compact 4.5 mm x 4.0 mm surface mount package configuration is designed to meet the tight lattice spacing requirements for phased array applications.

The QPF4006 is fabricated on Qorvo's 0.15um GaN on SiC process. It is housed in an air-cavity laminate package with an embedded copper heat slug. The copper slug, coupled with a low thermal resistance die-attach process, allows the QPF4006 to operate at the extreme case temperatures needed in phased array applications.



Functional Block Diagram



Product Features

- Frequency Range: 37 – 40.5 GHz
- RX Noise Figure: 4.2 dB
- RX Small Signal Gain: 18 dB
- RX Saturated Power: 17 dBm
- RX TOI : 20 dBm @ - 5 dBm Pin / tone
- TX Small Signal Gain: 23 dB
- TX Saturated Power: 33 dBm
- TX TOI: 42 dBm @ 24 dBm Pout / tone
- TX ACPR: 32dBc @ 24dBm average Pout [2]
- TX Linearity: 4% EVM @ 24 dBm average Pout [2]
- TX PAE: 7% @ 24 dBm average Pout.
- Package Dimensions: 4.5 x 4.0 x 1.8 mm

1. *Performance is typical at room temperature.*
2. *OFDM, 400 MHz modulation bandwidth, 64QAM.*

Applications

- 5G Wireless Base stations and terminals
- Point to Point Communications

Part No.	Description
QPF4006SR	Tape and Reel, Qty 100
QPF4006EVB03	QPF4006 Evaluation Board

Normal Operating Conditions

Parameter	Value
Drain Voltage	20 V
Drain Current (TXIDQ12 / TXIDQ3)	135 mA / 24 mA *
Drain Current (RX, IDQ)	15 mA
Gate Voltage (TXVG12/TXVG3)	−2 V / -2.4 V
Gate Voltage (RXVG)	-2 V
Control Voltage (TXSW, RXSW)	TXSW = 0 V, RXSW = 20V (RX on, TX off) TXSW = 20 V, RXSW = 0V (RX off, TX on)
Operating Temperature Range	−40 to 95 °C

Gate voltage shown are typical, can be adjusted to set required drain current. Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

* Other current settings: 45 / 60 mA = 105 mA; 90 / 120 mA = 210 mA; 135 / 180 mA = 315 mA (gate controls combined together).

Electrical Specifications RX

Test conditions, unless otherwise noted: VD = 20 V, IDQ = 15 mA. Data de-embedded to device reference planes, 25 °C

Parameter	Min	Typical	Max	Units
Frequency	37		40.5	GHz
Small Signal Gain		18		dB
Noise Figure		4.2		dB
Saturated Output Power		17		dBm
Input Return Loss		12		dB
Output Return Loss		15		dB
Output TOI, @ -5 dBm Pin / tone, 10 MHz tone spacing		20		dBm
Gain Temperature Coefficient		−0.056		dB/°C

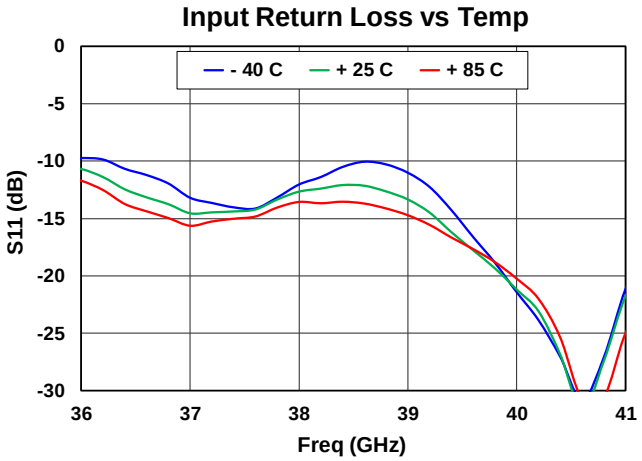
Electrical Specifications TX

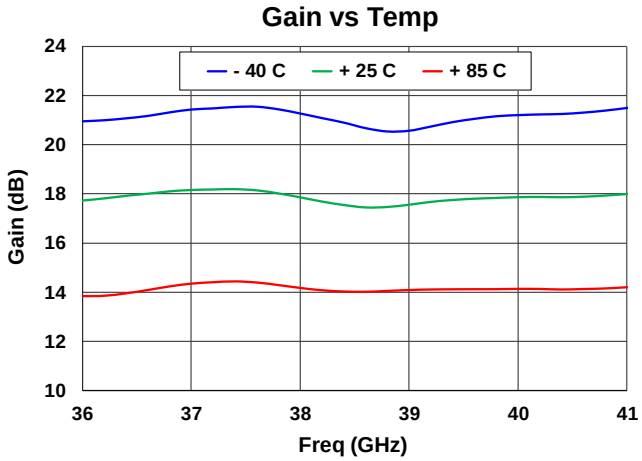
Test conditions unless otherwise noted: VD = 20 V, TXIDQ12 / TXIDQ3 = 135mA / 24 mA
Data de-embedded to device reference planes, 25 °C

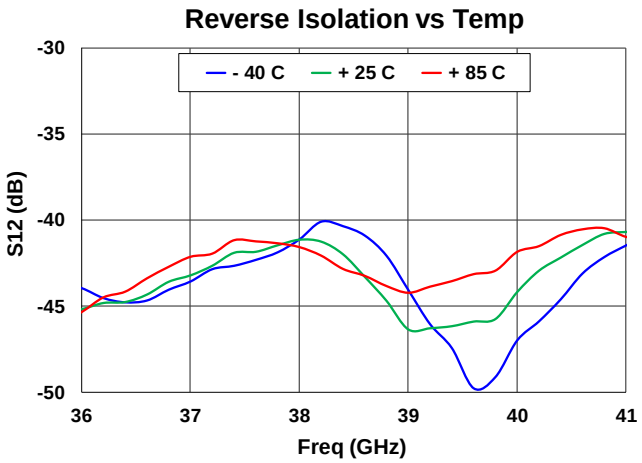
Parameter	Min	Typical	Max	Units
Frequency	37		40.5	GHz
Small Signal Gain		23		dB
Saturated Output Power		33		dBm
Input Return Loss		12		dB
Output Return Loss		13		dB
Output TOI, @ 24dBm Pout / tone, 10 MHz tone spacing		42		dBm
ACPR (24 dBm average power, OFDM, 400MHz, 64QAM)		-32		dBc
EVM (24 dBm average power, OFDM, 400MHz, 64QAM)		4		%
PAE at average output power (24dBm)		7		%
Gain Temperature Coefficient		−0.112		dB/°C

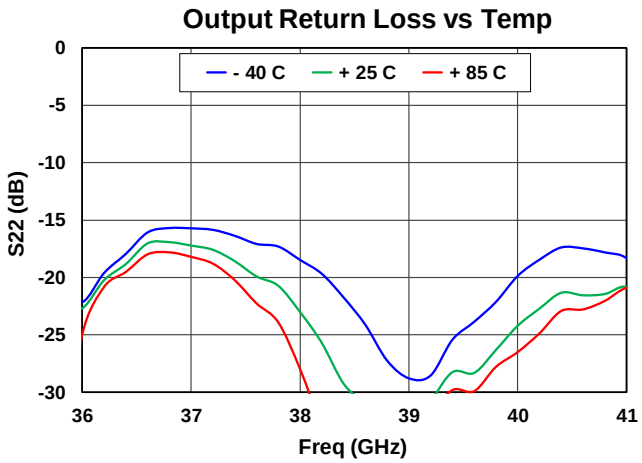
Performance Plots, Small Signal, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, Data de-embedded to device reference planes, 25C





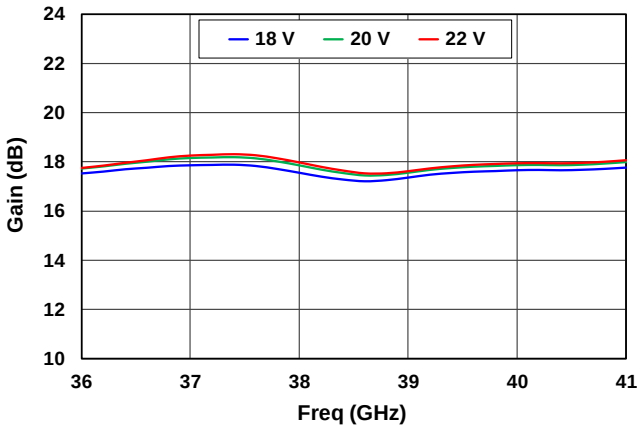




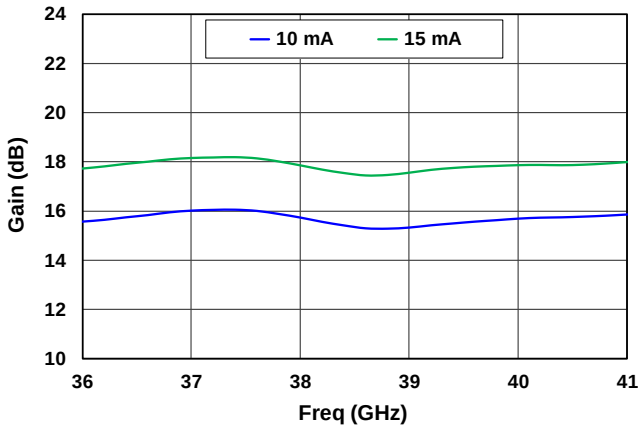
Performance Plots, Small Signal, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, Data de-embedded to device reference planes, 25 C

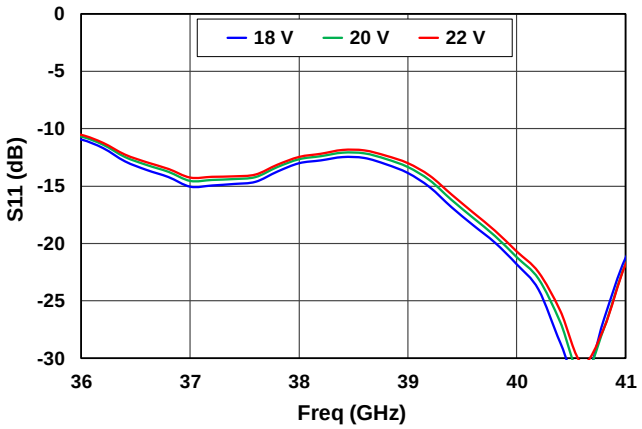
Gain vs Voltage



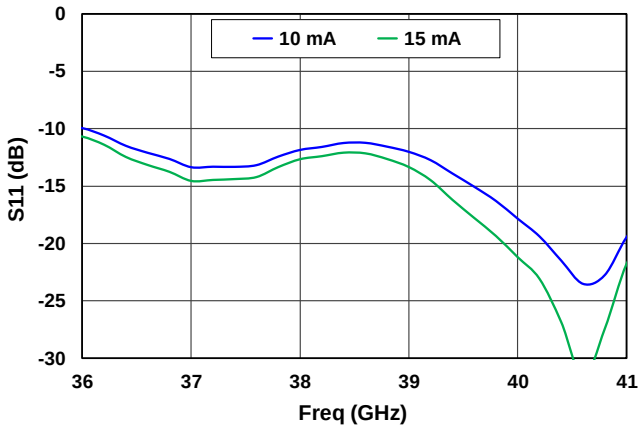
Gain vs Current



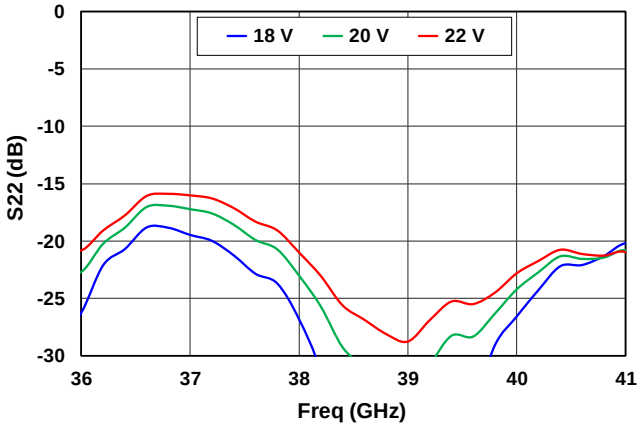
Input Return Loss vs Voltage



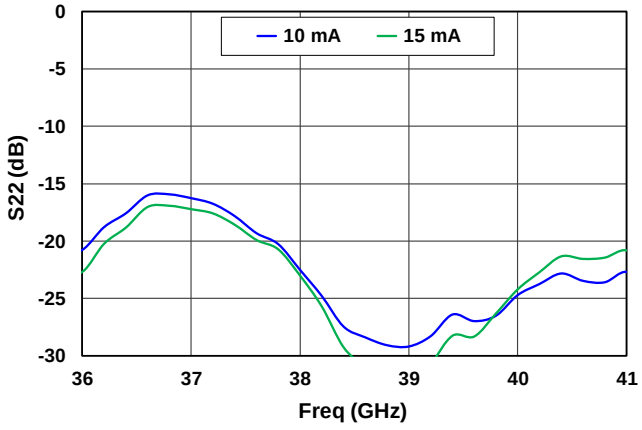
Input Return Loss vs Current



Output Return Loss vs Voltage

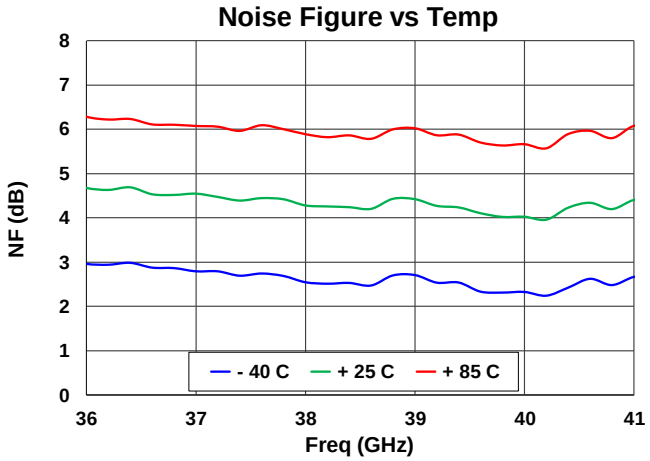


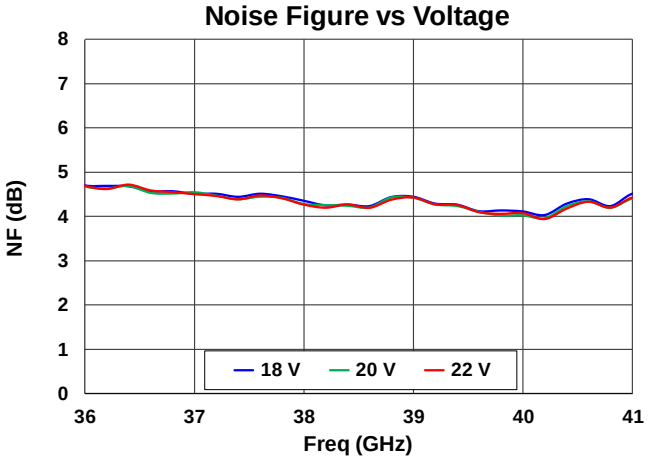
Output Return Loss vs Current

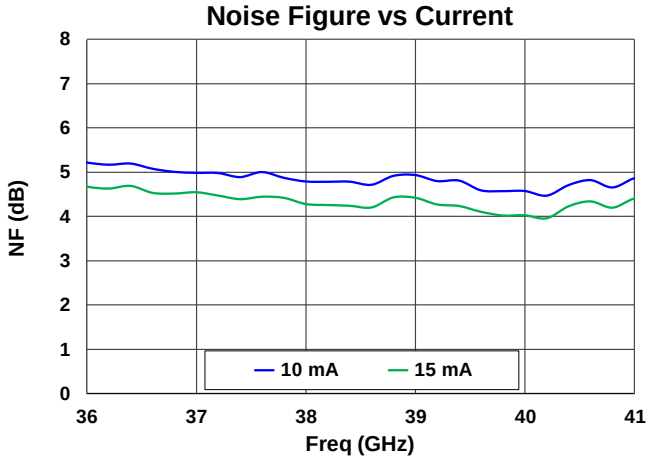


Performance Plots, Noise Figure, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, Data de-embedded to device reference planes, 25 C

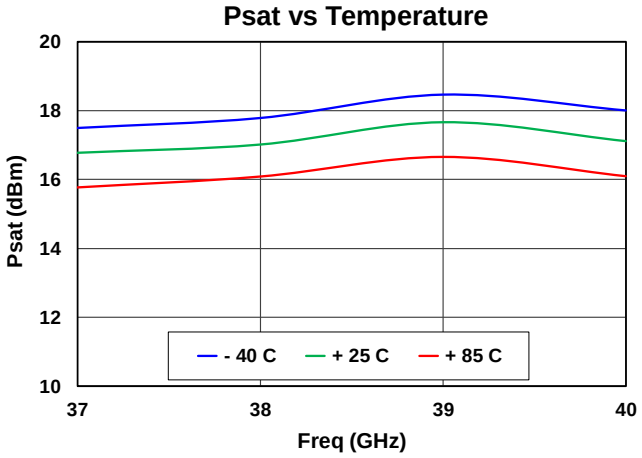


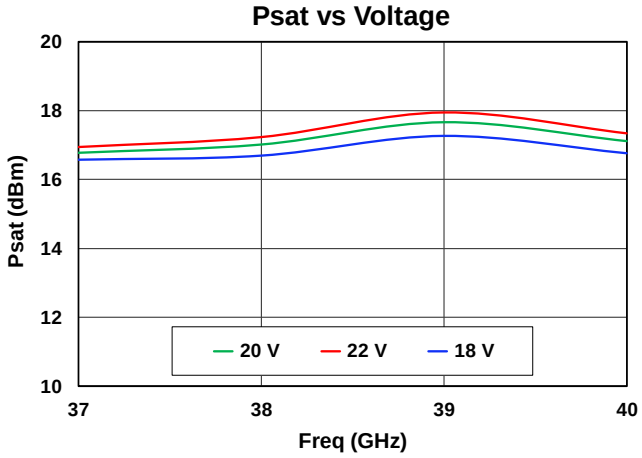


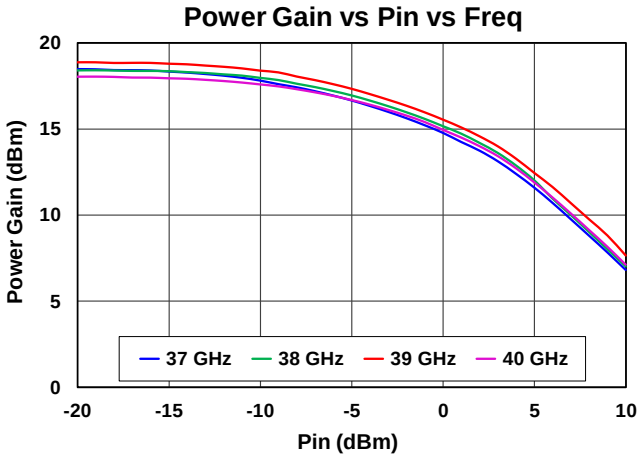


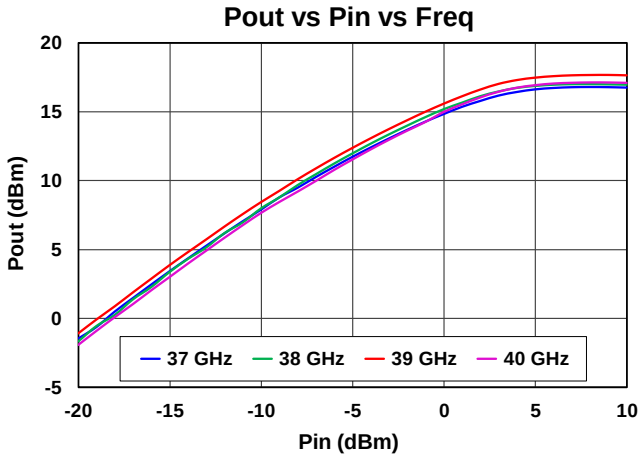
Performance Plots, Large Signal, Receive Path

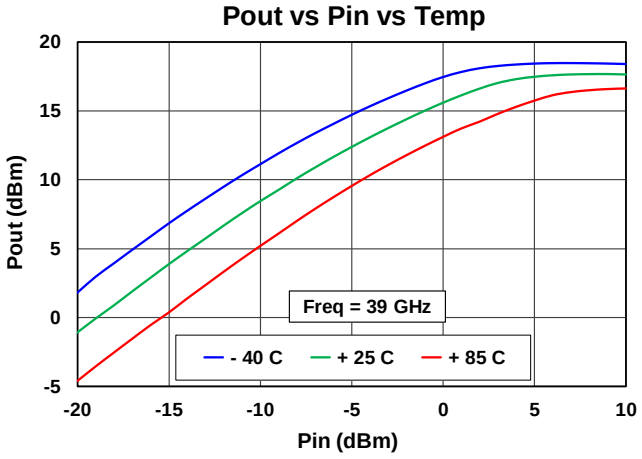
Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, CW. Data de-embedded to device reference planes, 25 C

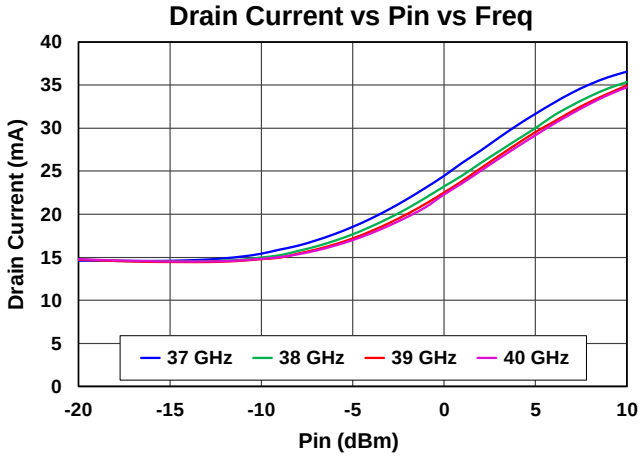






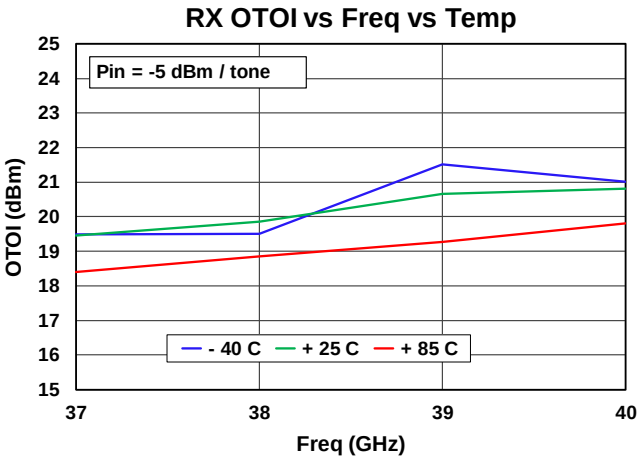


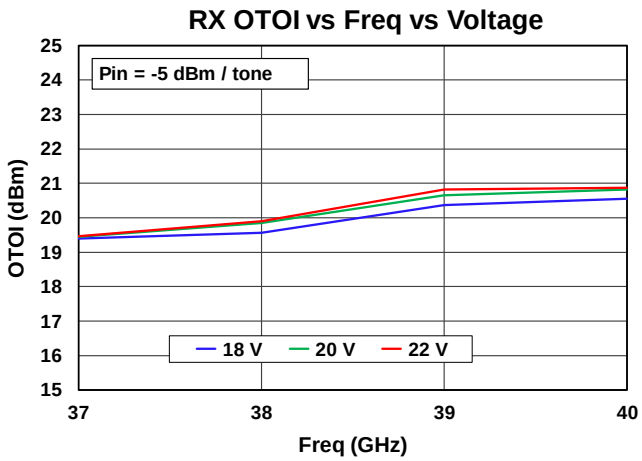


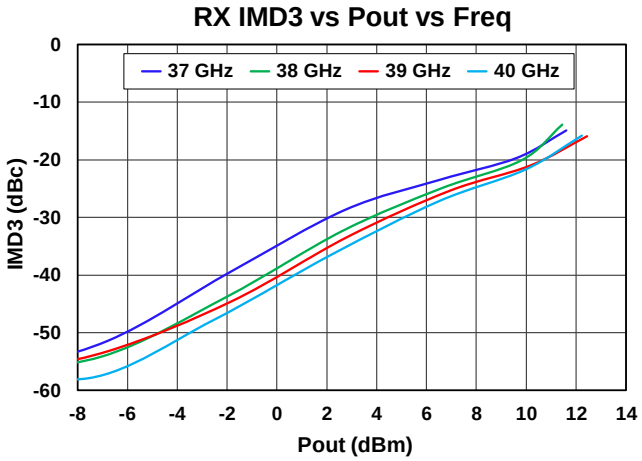


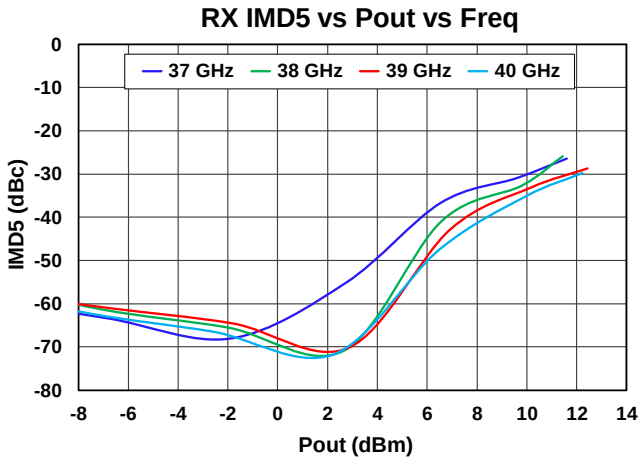
Performance Plots, Linearity, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, Tone spacing: 10 MHz
Data de-embedded to device reference planes, 25 C





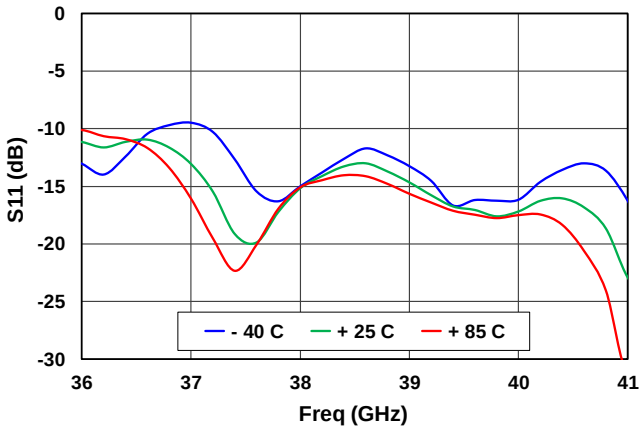




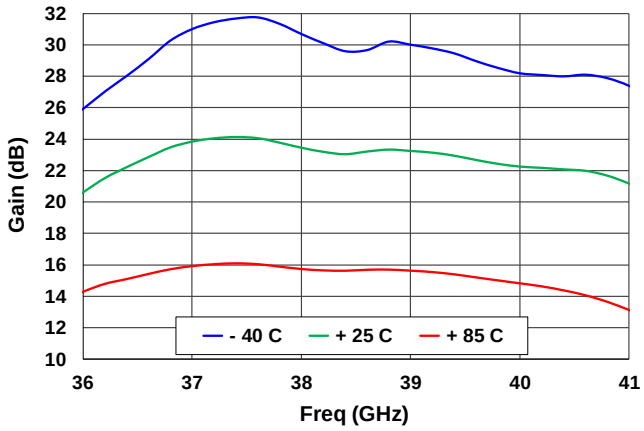
Performance Plots, Small Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA
Data de-embedded to device reference planes

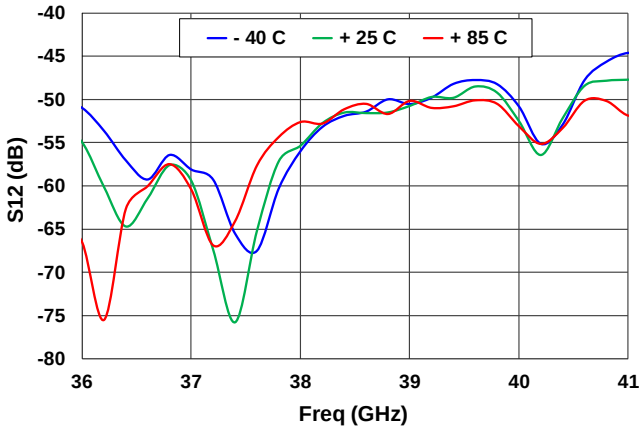
Input Return Loss vs Temp



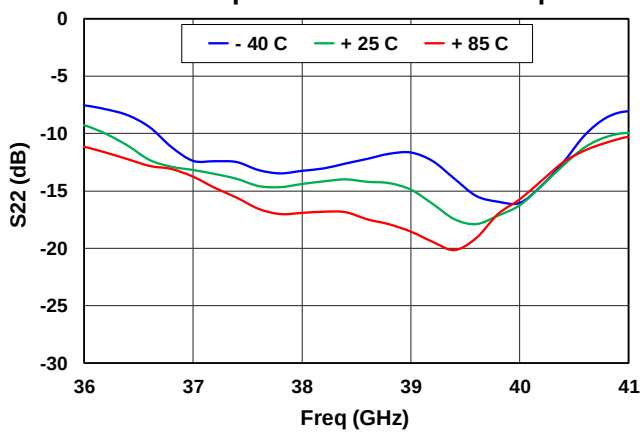
Gain vs Temp



Reverse Isolation vs Temp



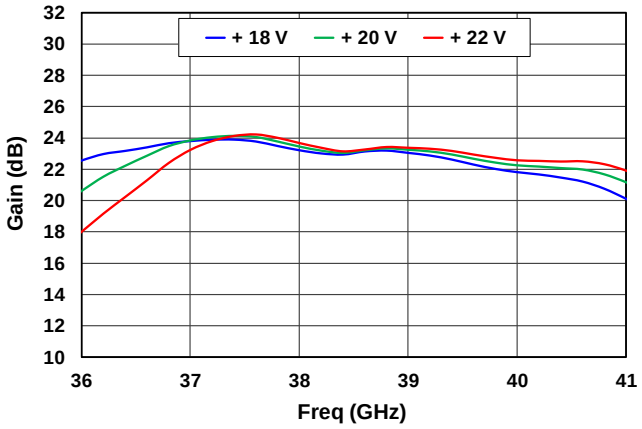
Output Return Loss vs Temp



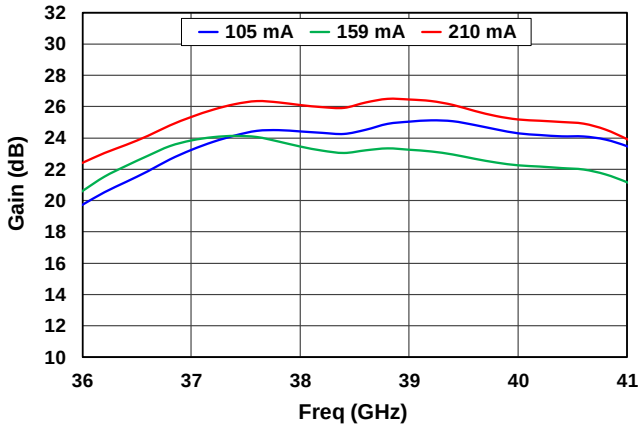
Performance Plots, Small Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA
Data de-embedded to device reference planes, 25 C

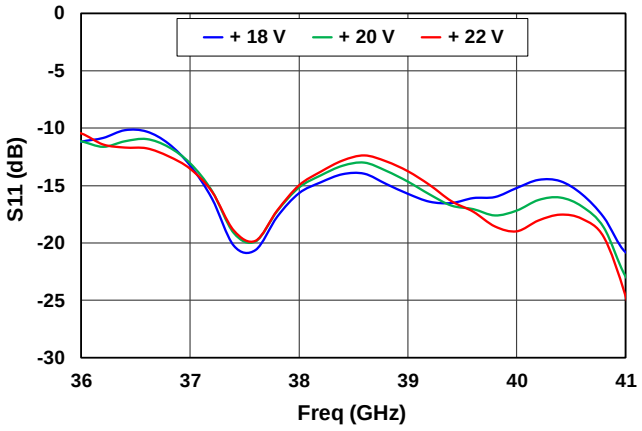
Gain vs Voltage



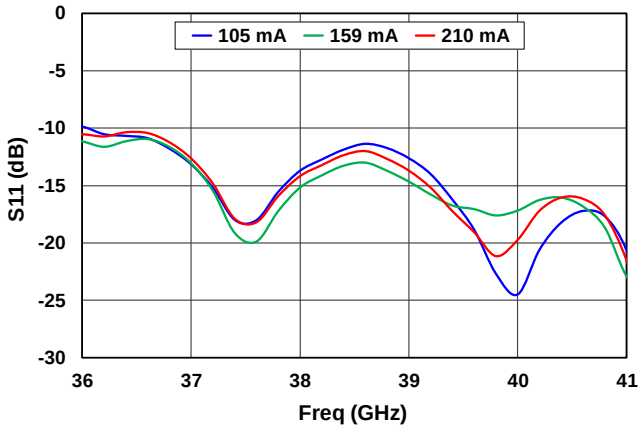
Gain vs Current



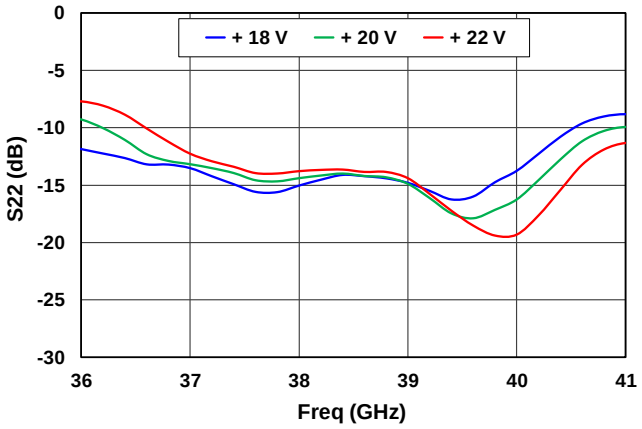
Input Return Loss vs Voltage



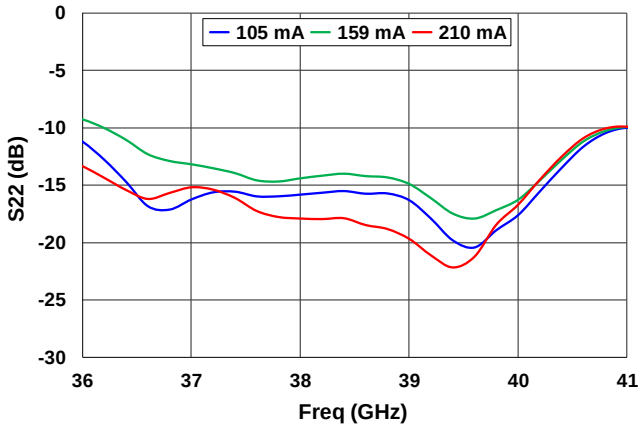
Input Return Loss vs Current



Output Return Loss vs Voltage

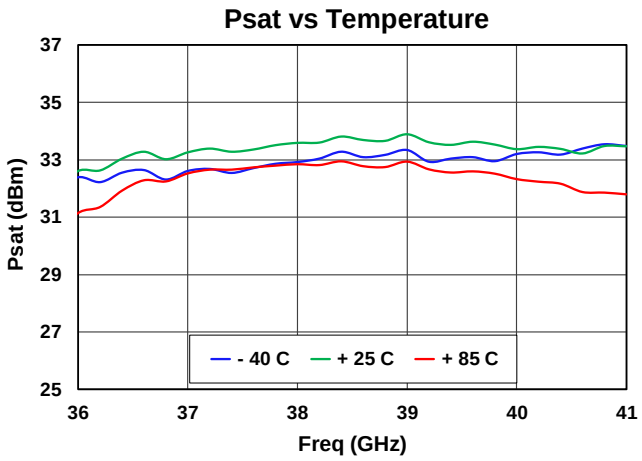


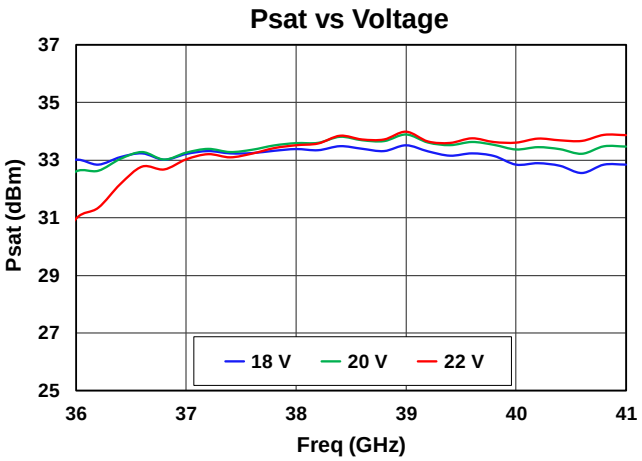
Output Return Loss vs Current

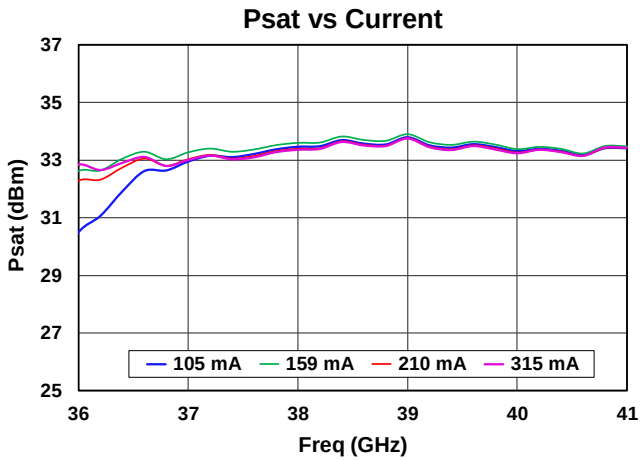


Performance Plots, Large Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, Pulse Mode: PW = 100 uS, DC = 10%
Data de-embedded to device reference planes, 25 C

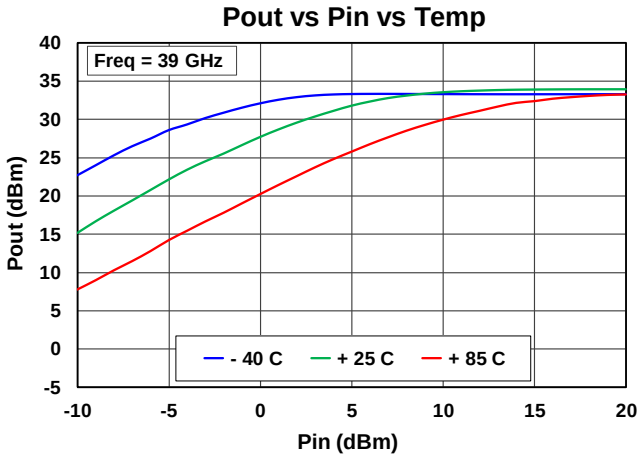


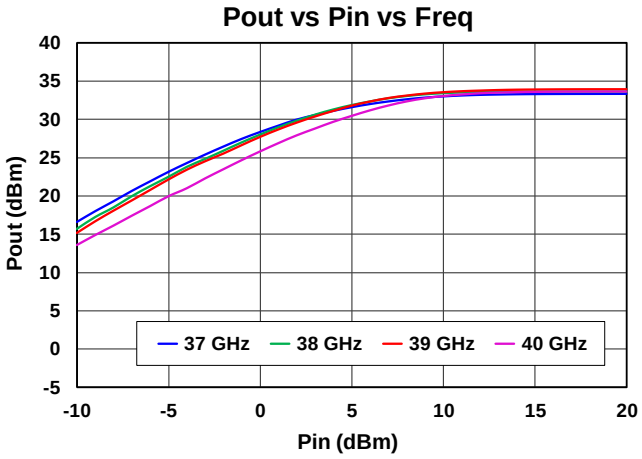


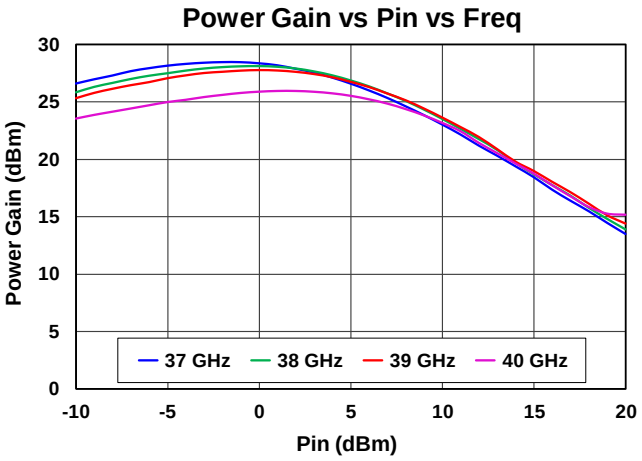


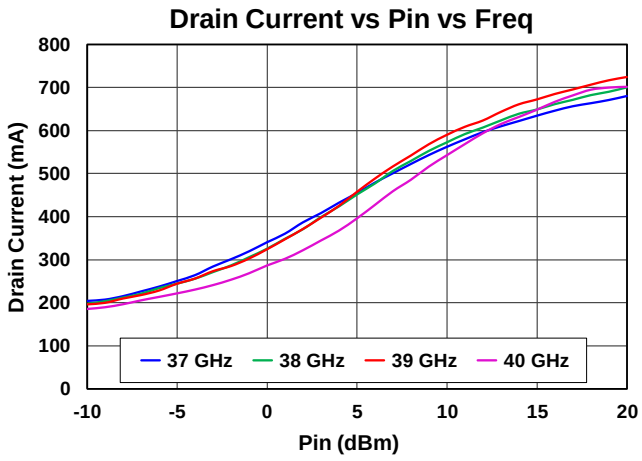
Performance Plots, Large Signal, Transmit Path

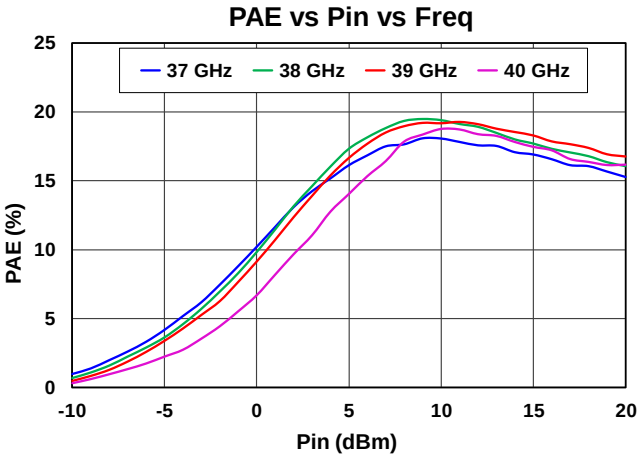
Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, Pulse Mode: PW = 100 uS, DC = 10%
Data de-embedded to device reference planes. 25C

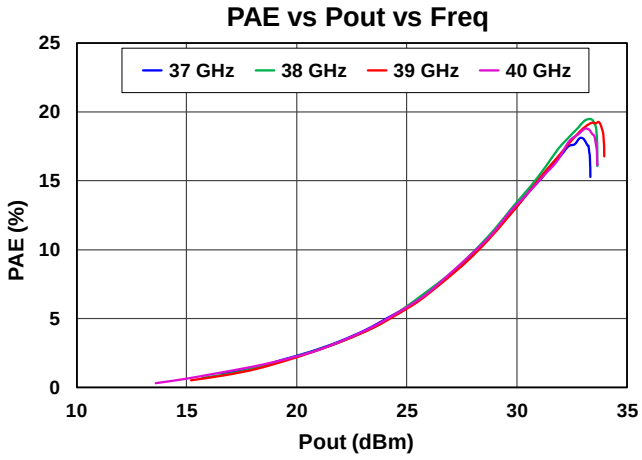






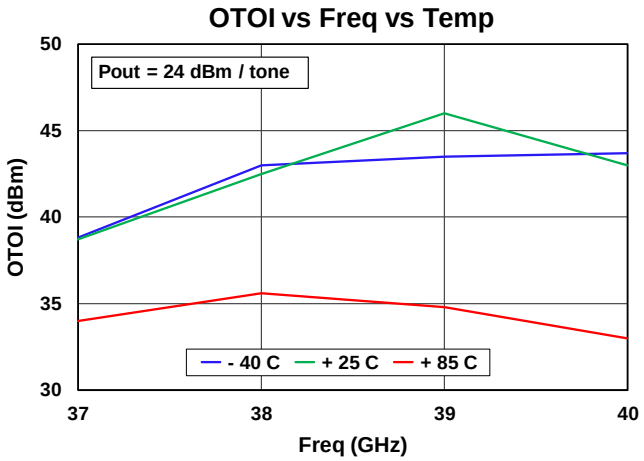


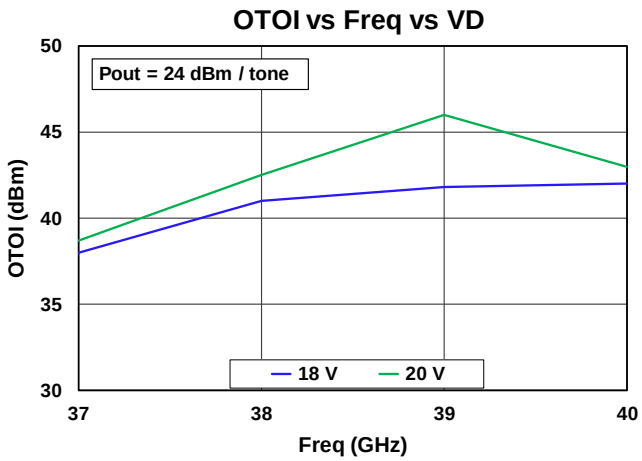


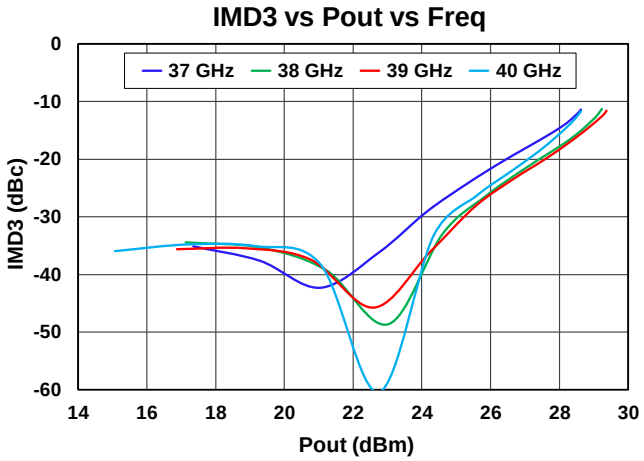


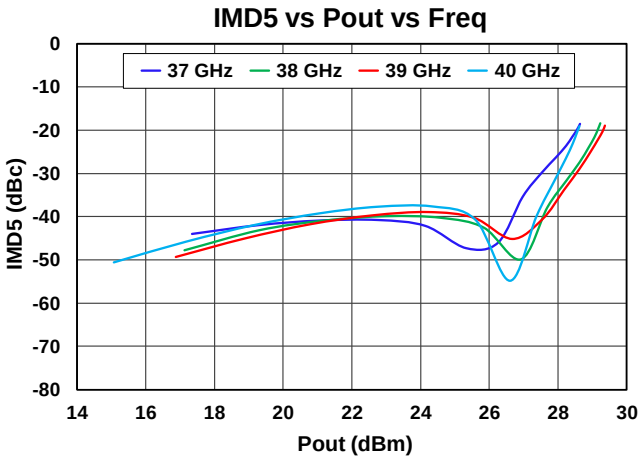
Performance Plots, Linearity, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, Tone Spacing = 10 MHz
Data de-embedded to device reference planes, 25 C





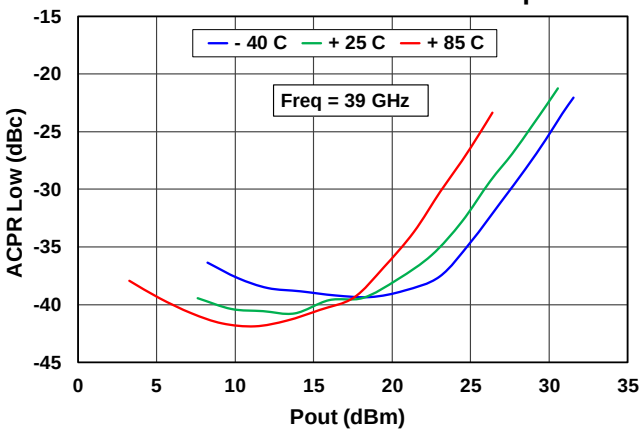




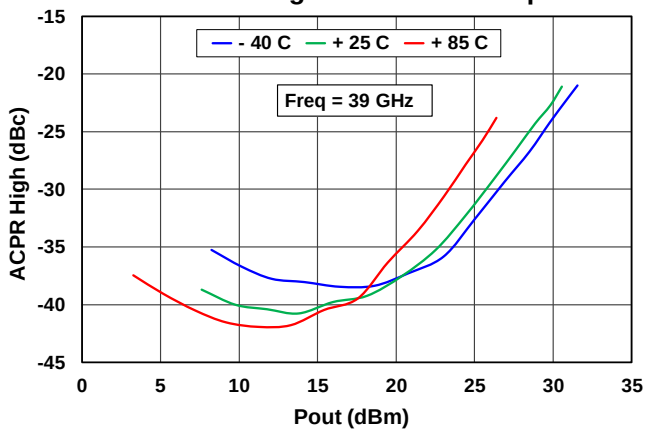
Performance Plots, Modulated Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, Source: 400 MHz OFDM, 64 QAM
Data de-embedded to device reference planes, 25 C

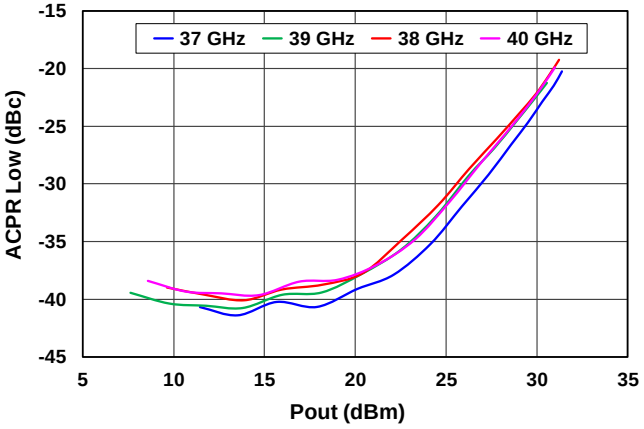
ACPR Low vs Pout vs Temp



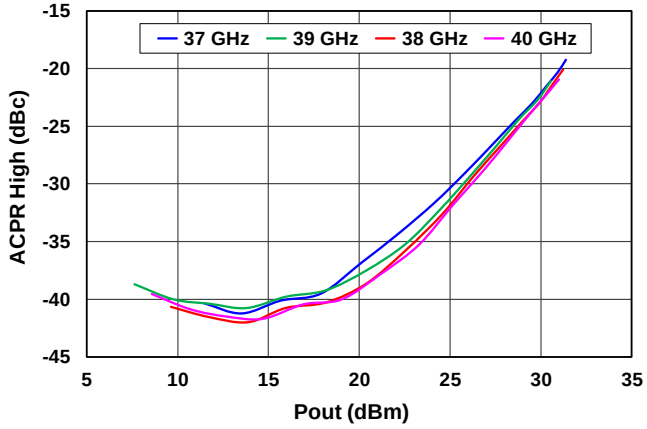
ACPR High vs Pout vs Temp



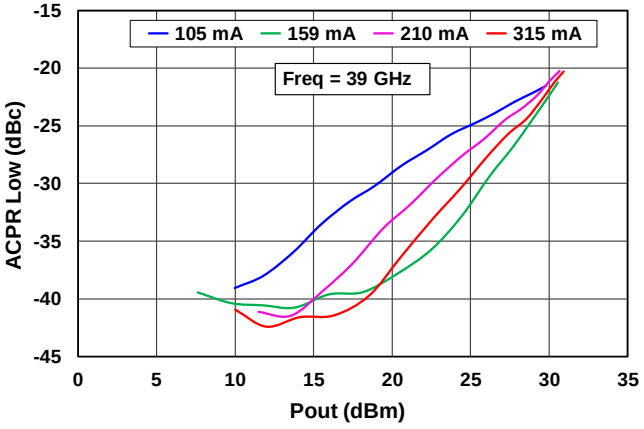
ACPR Low vs Pout vs Freq



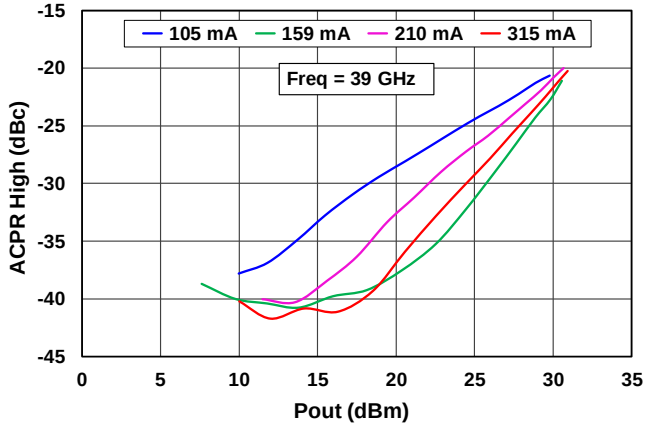
ACPR High vs Pout vs Freq



ACPR Low vs Pout vs Current

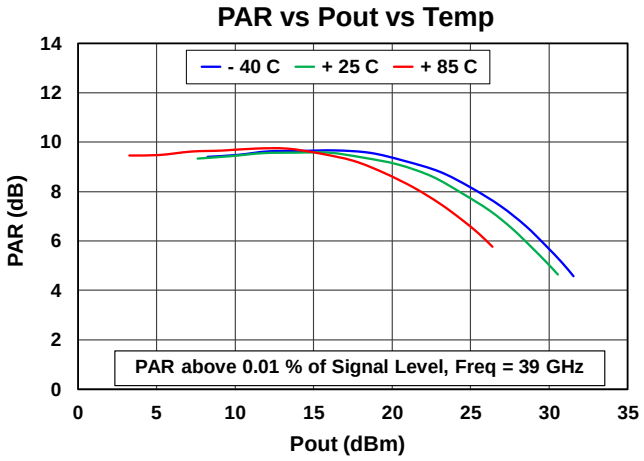


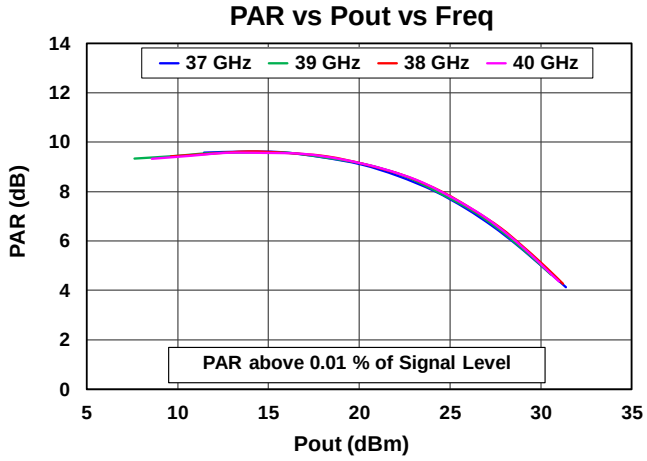
ACPR High vs Pout vs Current

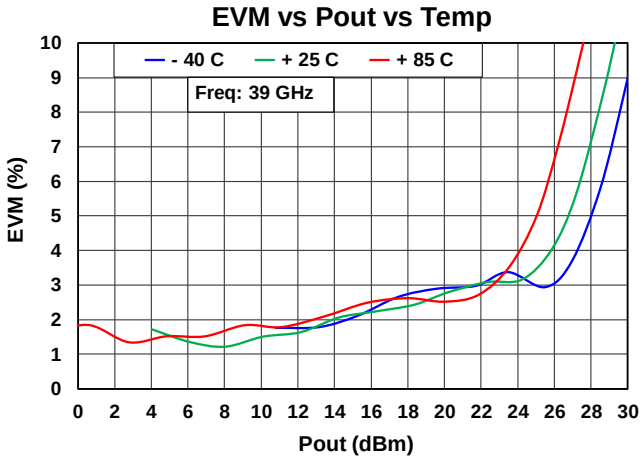


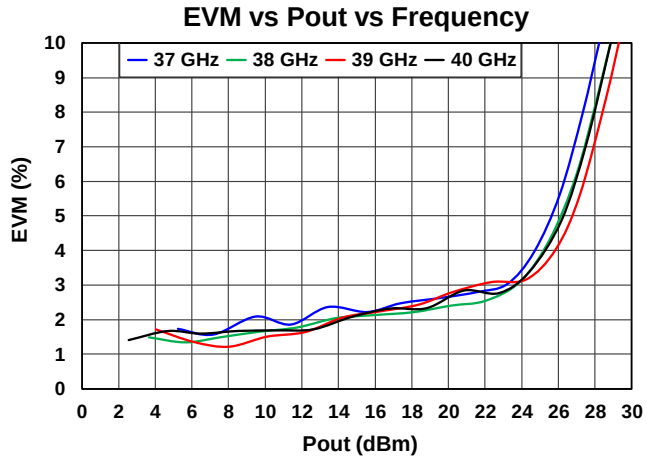
Performance Plots, Modulated Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, Source: 400 MHz OFDM, 64 QAM
Data de-embedded to device reference planes, 25 C



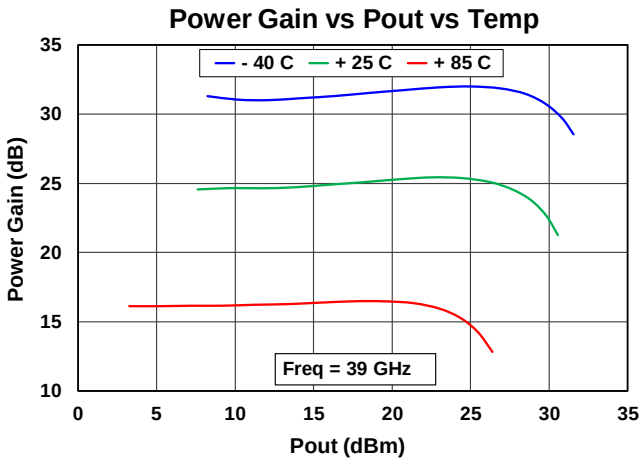


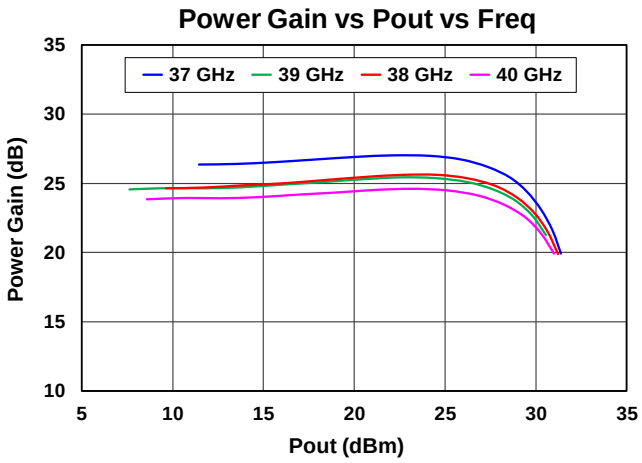


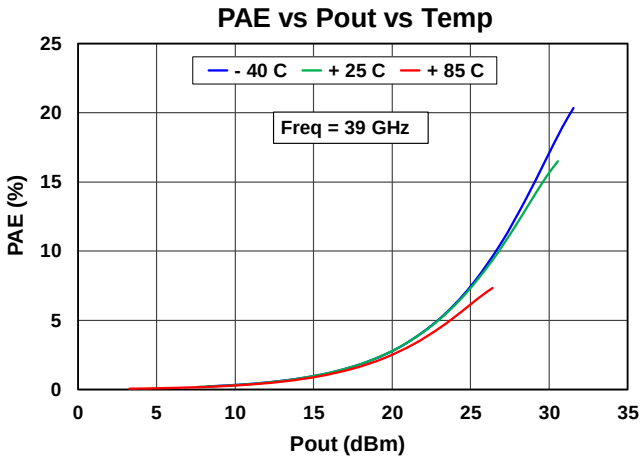


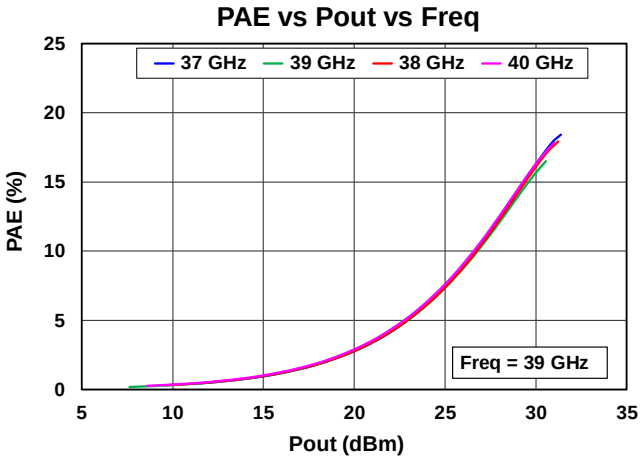
Performance Plots, Modulated Signal, Transmit Path

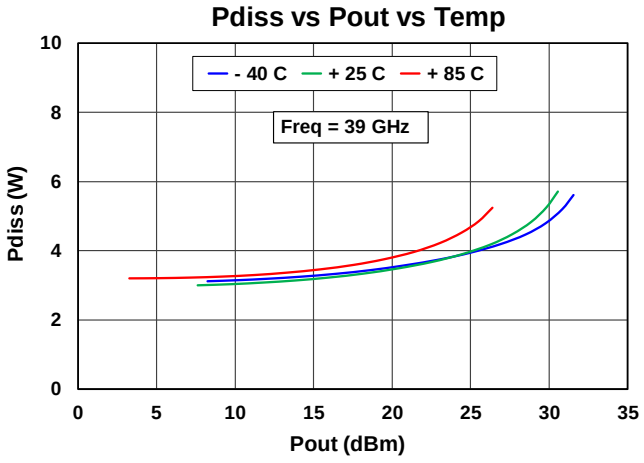
Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, Source: 400 MHz OFDM, 64 QAM
Data de-embedded to device reference planes, 25 C

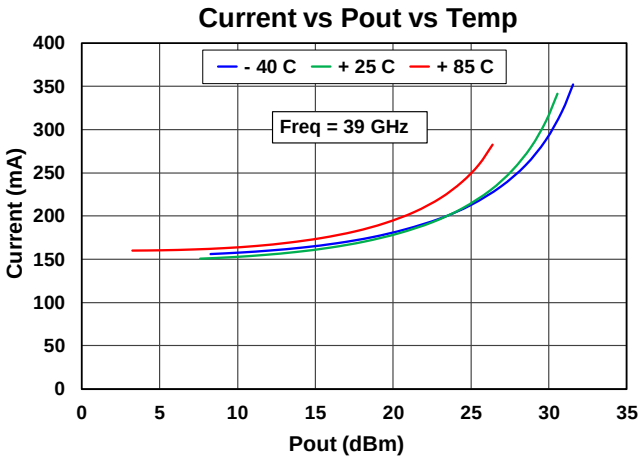




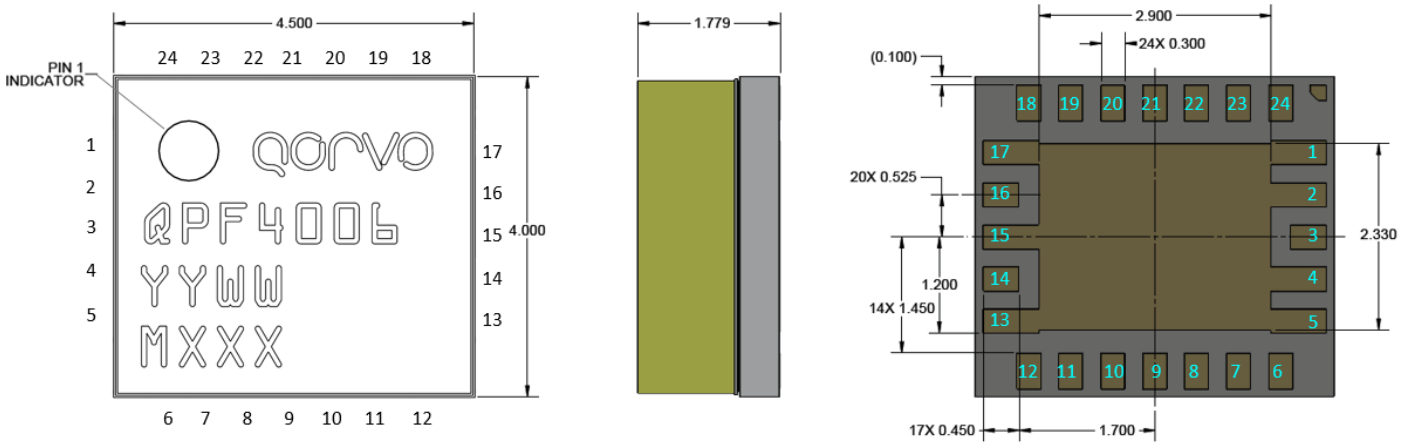








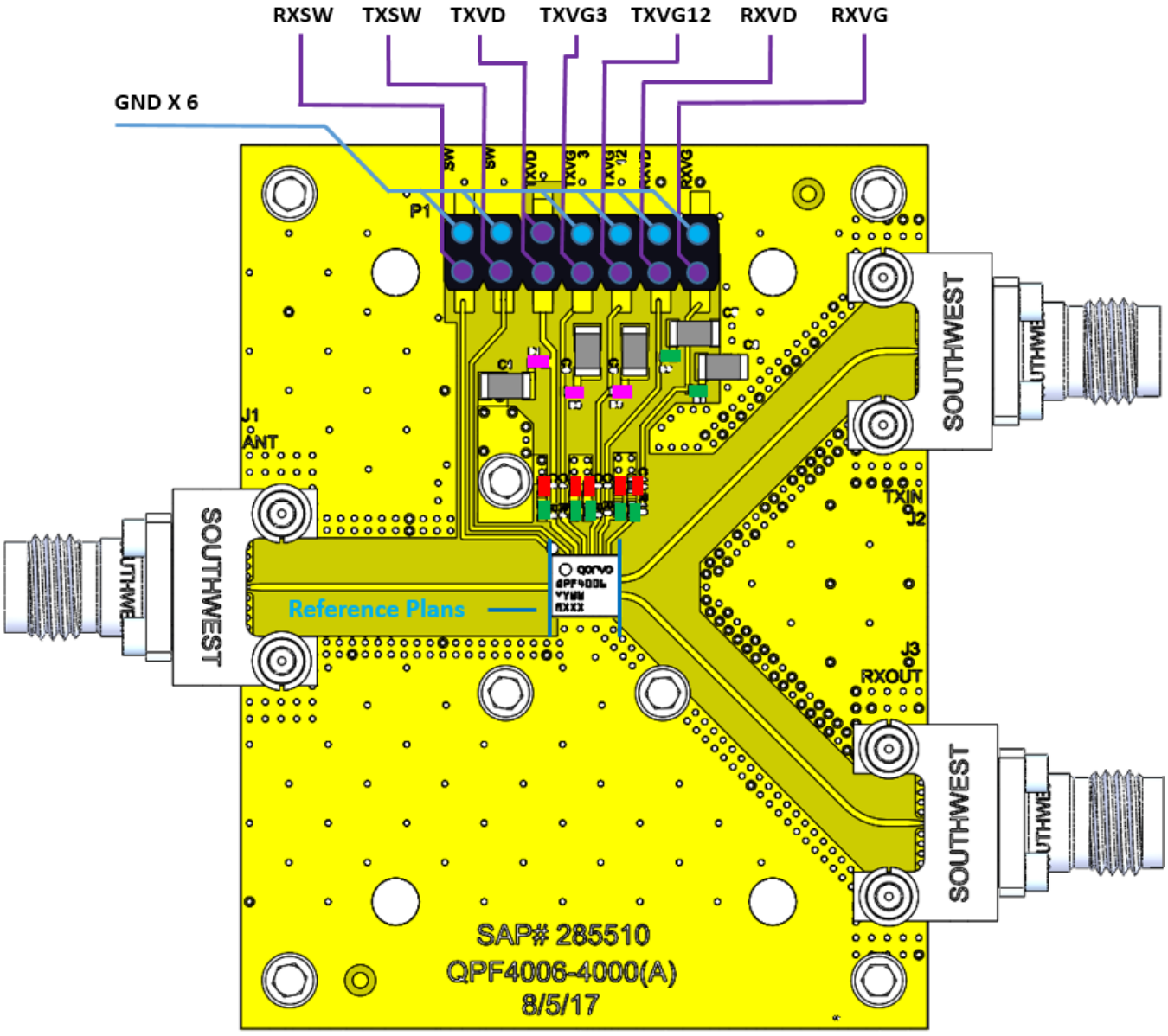
Mechanical Drawings & Pad Descriptions



Dimensions in mm
Part Marking:
QPF4006: Part Number
YY = Part Assembly Year
WW = Part Assembly Week
MXXX = Batch ID

Pin Number	Label	Description
1, 2, 4, 5, 13, 15, 17, slug	GND	GROUND
3	ANT	Antenna
14	RXOUT	Receive output
16	TXIN	Transmit input
18	RXVG	Receive gate control
19	RXVD	Receive Drain Voltage
20	TXVG12	Transmit stage 1 and 2 gate controls
21	TXVG3	Transmit stage 3 gate control
22	TXVD	Transmit Drain Voltage
23	TXSW	Transmit switch control
24	RXSW	Receive switch control
6, 7, 8, 9, 10, 11, 12	N/C	No internal connection

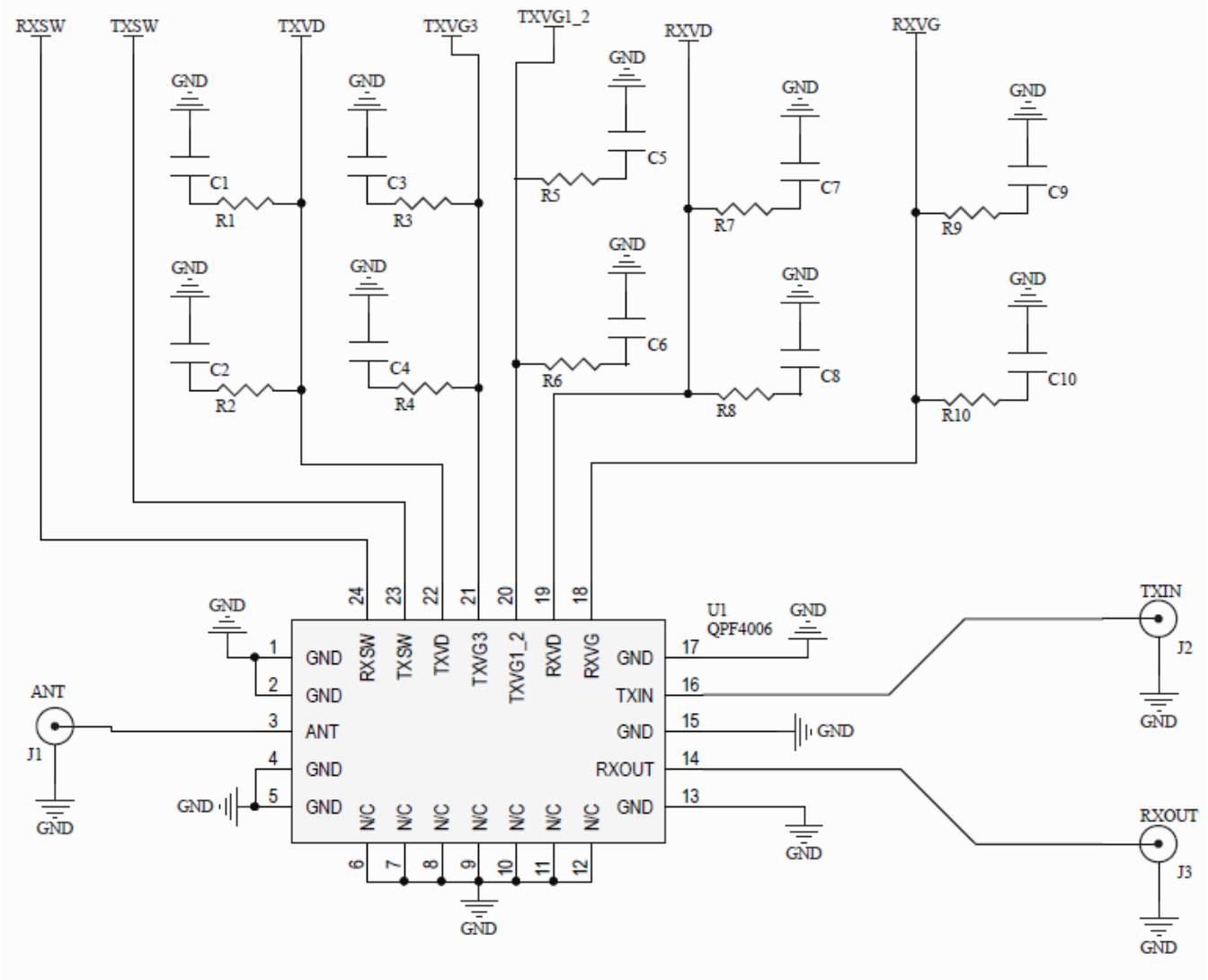
Evaluation Board and Assembly



RF Layer is 0.008" thick Rogers Corp. RO4003C (ε_r = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1492-04A-5.

Ref. Des.	Component	Value	Manuf.	Remark
C2, C4, C6, C8, C10	SMT Cap.	CAP, 0402 1000pF +/-10% 50V 0402 X7R ROHS	Various	Red
C1, C3, C5, C7, C9	SMT Cap.	CAP, 1206 1.0uF +/-10% 50V X7R ROHS	Various	Grey
R2, R4, R6 - R10	SMT Res.	RES, 0402 5.1 OHM, 5% 50V, ROHS	Various	Green
R1, R3, R5	SMT Res.	RES, 0402 0 OHM, 5%, ROHS	Various	Pink

Application Circuit



Bias-up Procedure

1. Set drain supply TXVD limit to 700 mA, RXVD limit to 50 mA, gate and control supply limit to 10 mA each.
2. Set TXVG12, TXVG3, RXVG to −5 V
3. Set TXSW = 20 V (or 0 V), RXSW = 0 V (or 20 V)
4. Set VD = +20 V
5. For TX, adjust TXVG12 to get TXID12 current, then adjust TXVG3 to achieve required total drain current; For RX, adjust RXVG to achieve required drain current.
6. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Set TXVG12, TXVG3 and RXVG to −5 V
3. Set VD = 0 V
4. Turn off drain supply
5. Turn off TXSW, RXSW
6. Turn off gate supply

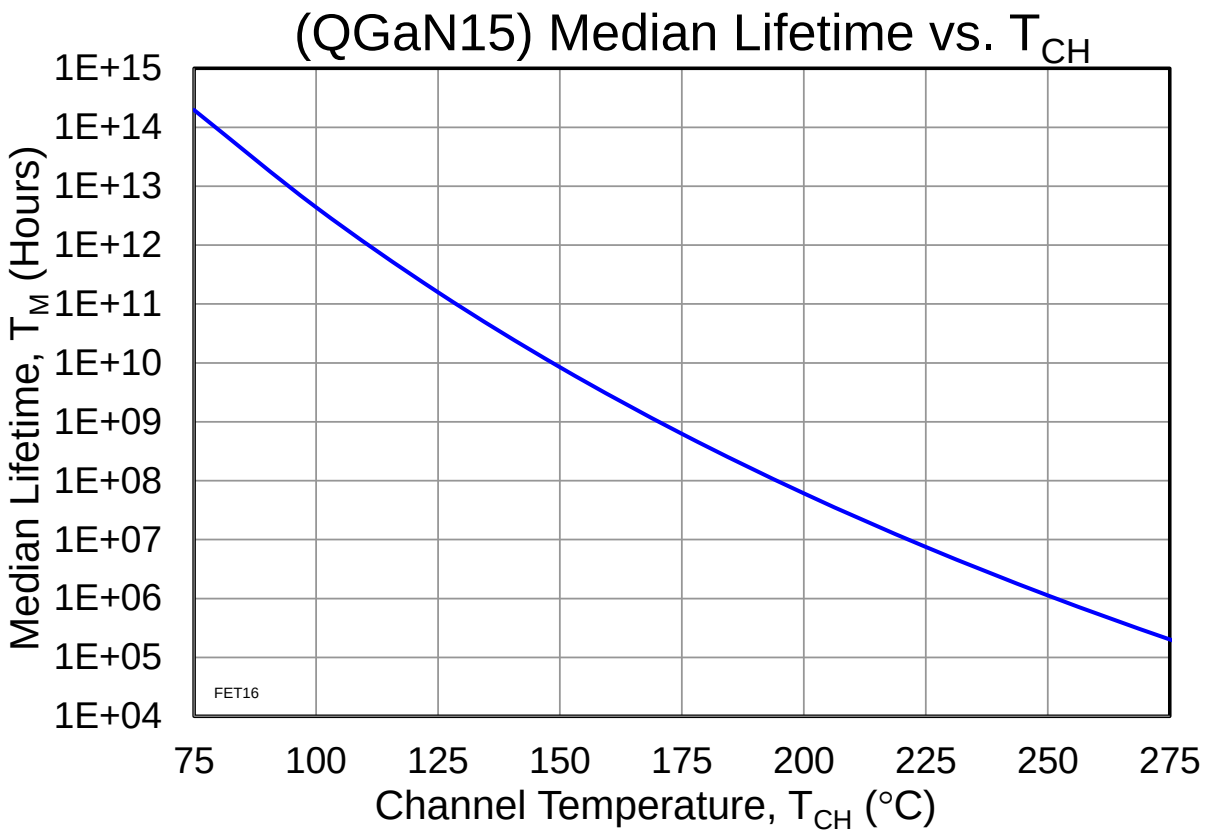
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	TX on, RX off, CW, V_D = +20 V, I_{DQ} = 159 mA, T_{BASE} = 85 °C, RF off, P_{DISS} =3.18 W	18.68	°C/W
Channel Temperature (T_{CH}) (Quiescent)		154.38	°C
Median Lifetime (T_M)		5.3E+9	Hrs
Thermal Resistance (θ_{JC}) (1)	TX on, RX off, CW, V_D = +20 V, I_{DQ} = 159 mA, T_{BASE} = 85 °C, Freq = 39 GHz, P_{IN} = 10 dBm, P_{OUT} = 25 dBm, P_{DISS} = 4.69 W, I_{D_Drive} = 0.25 A	13.6	°C/W
Channel Temperature (T_{CH}) (under RF drive)		158.84	°C
Median Lifetime (T_M)		3.3E+9	Hrs
Thermal Resistance (θ_{JC}) (1)	RX on, TX off, CW, V_D = +20 V, I_{DQ} = 15 mA, T_{BASE} = 85 °C, RF off, P_{DISS} = 0.3 W	66.67	°C/W
Channel Temperature (T_{CH}) (Quiescent)		115	°C
Median Lifetime (T_M)		5.7E+11	Hrs

Notes:
1. Thermal resistance measured to back of package.

Median Lifetime

Test Conditions: V_D = +28 V; Failure Criteria = 10 % reduction in ID_MAX during DC Life Testing



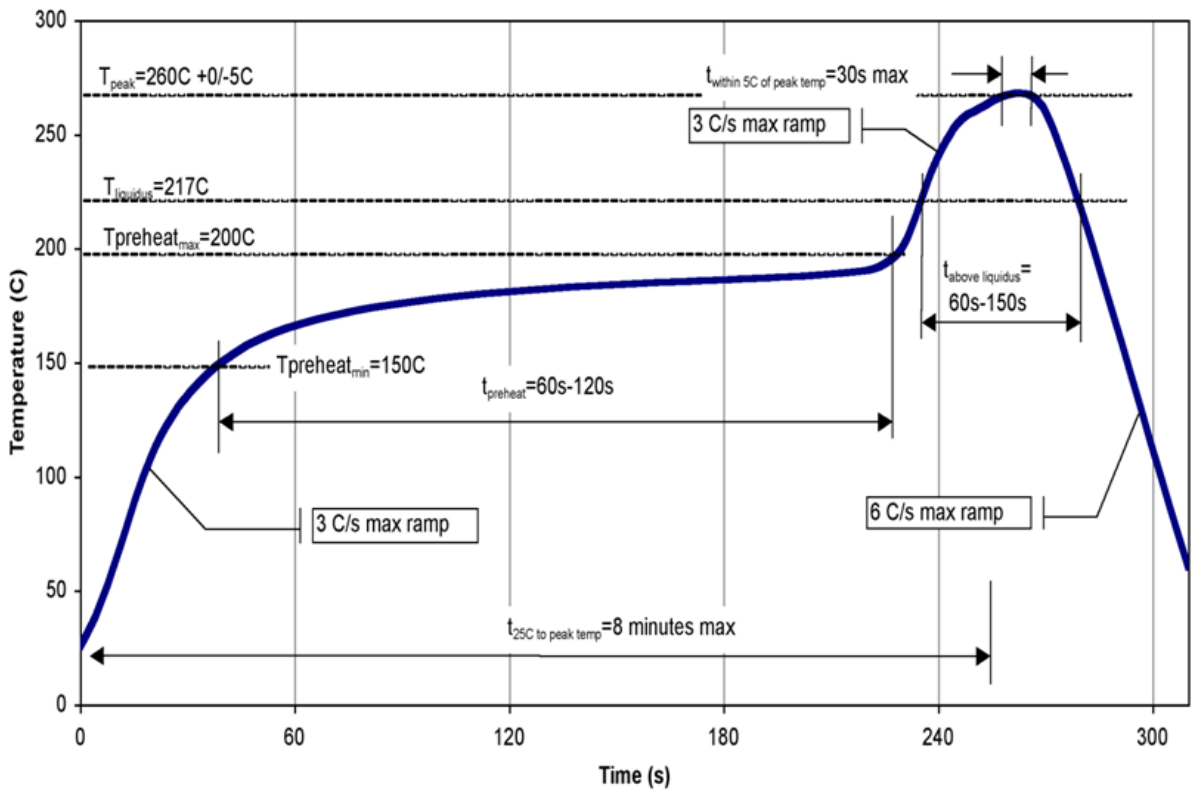
Absolute Maximum Ratings

Parameter	Value
Drain Voltage (TXVD, RXVD)	28 V
Drain Current (TXID3+TXID12)	800 mA
Drain Current (RXID)	60 mA
Gate Voltage (RXVG, TXVG3, TXVG12)	0 to −5 V
Gate Current (RXIG, TXIG3, TXIG12)	20 mA
Switch Control Voltage (TXSW, RXSW)	0 to 28 V
Switch Control Current	20 mA
RF Input Power (All RF ports, 85 °C)	30 dBm
Channel Temperature, T_{CH}	225 °C
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Solderability and Recommended Soldering Profile

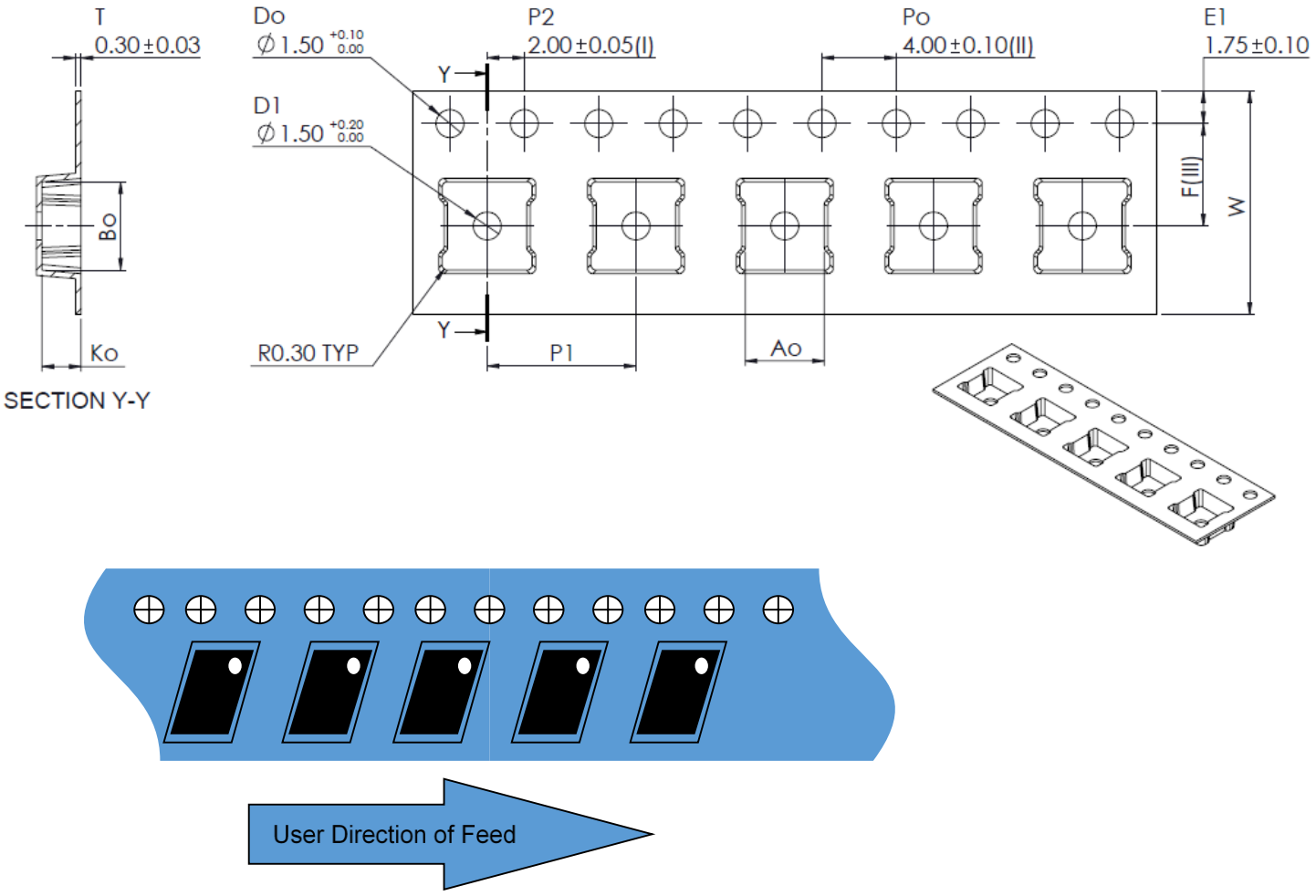
1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.
2. The use of no-clean solder to avoid washing after soldering is recommended.



Tape and Reel Information

Standard T/R size = 100 pieces on a 7” reel.

Material		Cavity (mm)				Distance Between Centerline (mm)		Carrier Tape (mm)	Cover Carrier (mm)
Vendor	Vendor P/N	Length (A0)	Width (B0)	Depth (K0)	Pitch (P1)	Length direction (P2)	Width Direction (F)	Width (W)	Width (W)
Tek-Pak	QFN0400X 0450C	4.25	4.75	2.1	8.0	2.00	5.50	12.0	9.20



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	TBD	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	TBD	JEDEC standard IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: 1-844-890-8163

Web: www.qorvo.com

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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