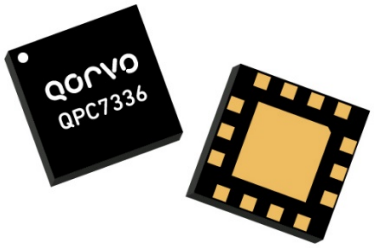
QPC7336

45MHz to 1218MHz Variable Equalizer

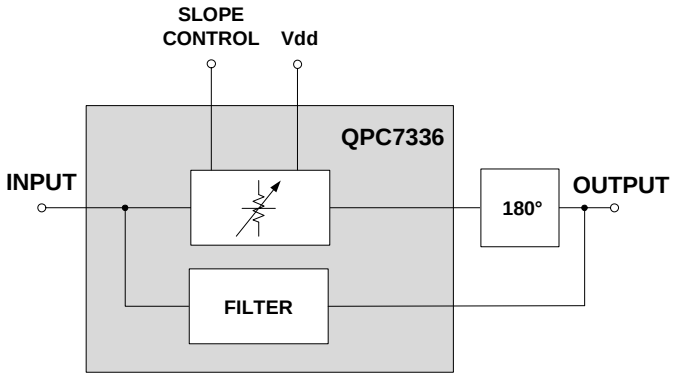
Product Description

The QPC7336 is a voltage controlled variable equalizer employing SOI attenuator, optimized for DOCSIS 3.1 operation between 45MHz and 1218MHz.



14 pin, 6.0 mm x 6.0 mm x 1.375 mm package

Functional Block Diagram



Product Features

- 45 – 1218 MHz Operational Bandwidth
- 10dB slope range
- Low insertion loss
- High linearity
- 75Ohm impedance for CATV applications
- 5V single supply voltage
- Low power consumption
- Positive or negative slope control gradient

Applications

CATV amplifier and transmission systems

Ordering Information

Part No.	Description
QPC7336SB	Sample bag 5 pcs
QPC7336SQ	Sample bag 25 pcs
QPC7336SR	7” Reel with 100 pcs
QPC7336TR7	7” Reel with 500 pcs
QPC7336TR13	13” Reel with 1000 pcs
QPC7336PCBA-410	Fully assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Supply Voltage (Vdd)	-0.5 to +6V
Control Voltage (Vc)	-0.5 to +6V
Control Voltage 2 (Vc2)	-2 to +24V
MODE	-0.5 to +6V
Storage Temperature	−40 to 100 °C
RF Input Power	+30 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (Vdd)		+5		V
Junction Temperature			+125	°C
Operating Temperature	-30		+100	°C

Electrical specifications are measured at specified test conditions in application circuit. Specifications are not guaranteed over all recommended operating conditions.

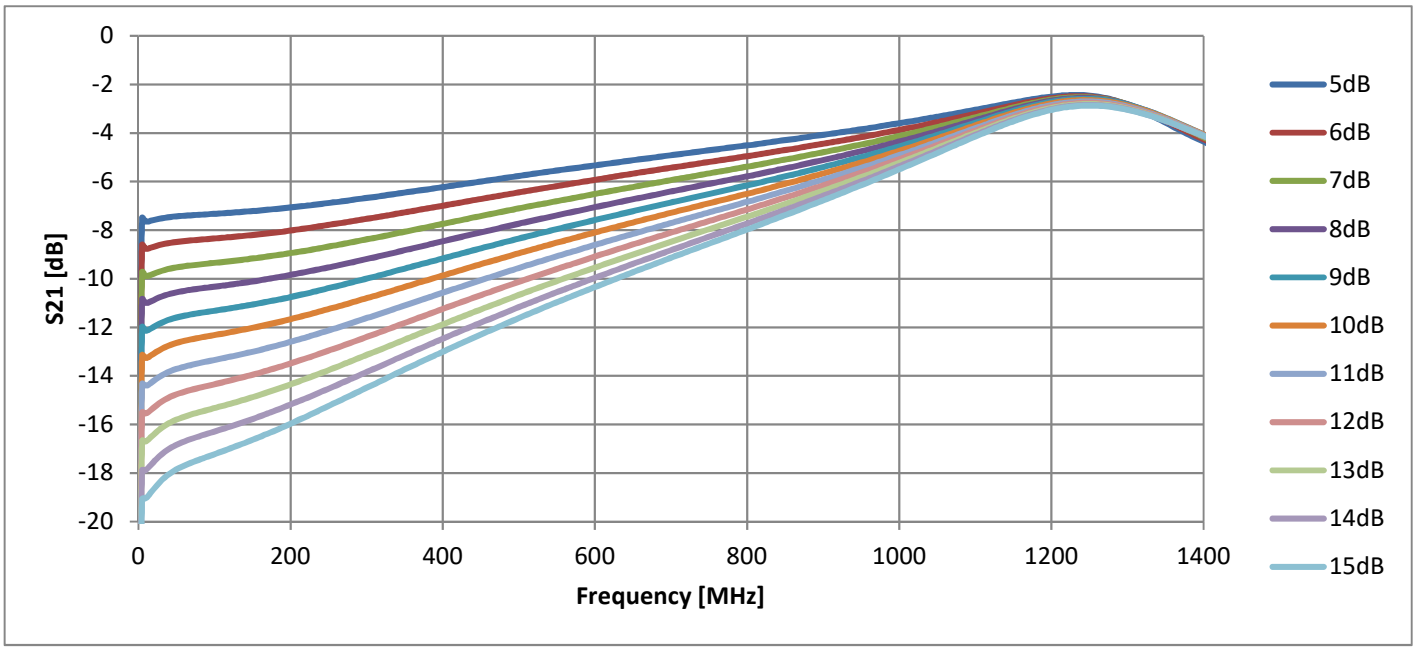
Electrical Specifications – Tested in Evaluation Circuit

Parameter	Conditions (Vdd=5V, T_{MB}=25°C, Z_S=Z_L=75Ω)	Min	Typ	Max	Units
General Performance					
Supply Current (I_{dd})			2		mA
Thermal Resistance			70		K/W
RF Input Power				27	dBm
RF Performance					
Frequency Range		45		1218	MHz
Insertion Loss (S21)	f= 1218MHz, slope set between 5dB and 15dB		2.75	3.0	dB
Minimum Slope [1]	f= 45 to 1218MHz		1		dB
Maximum Slope [1]	f= 45 to 1218MHz		20		dB
Flatness [2]	f= 45 to 1218MHz, slope set between 5dB and 15dB		0.6		dB
Input Return Loss (S11)	slope set between 5dB and 15dB		-16		dB
Output Return Loss (S22)	slope set between 5dB and 15dB		-16		dB
Input IP3	P_{IN} + ($IM3_{dBc}$/2) 6MHz tone spacing at 15dBm/tone		50		dBm
Input IP2	P_{IN} + $IM2_{dBc}$, IM2 is F1 + F2 6MHz tone spacing at 15dBm/tone		80		dBm

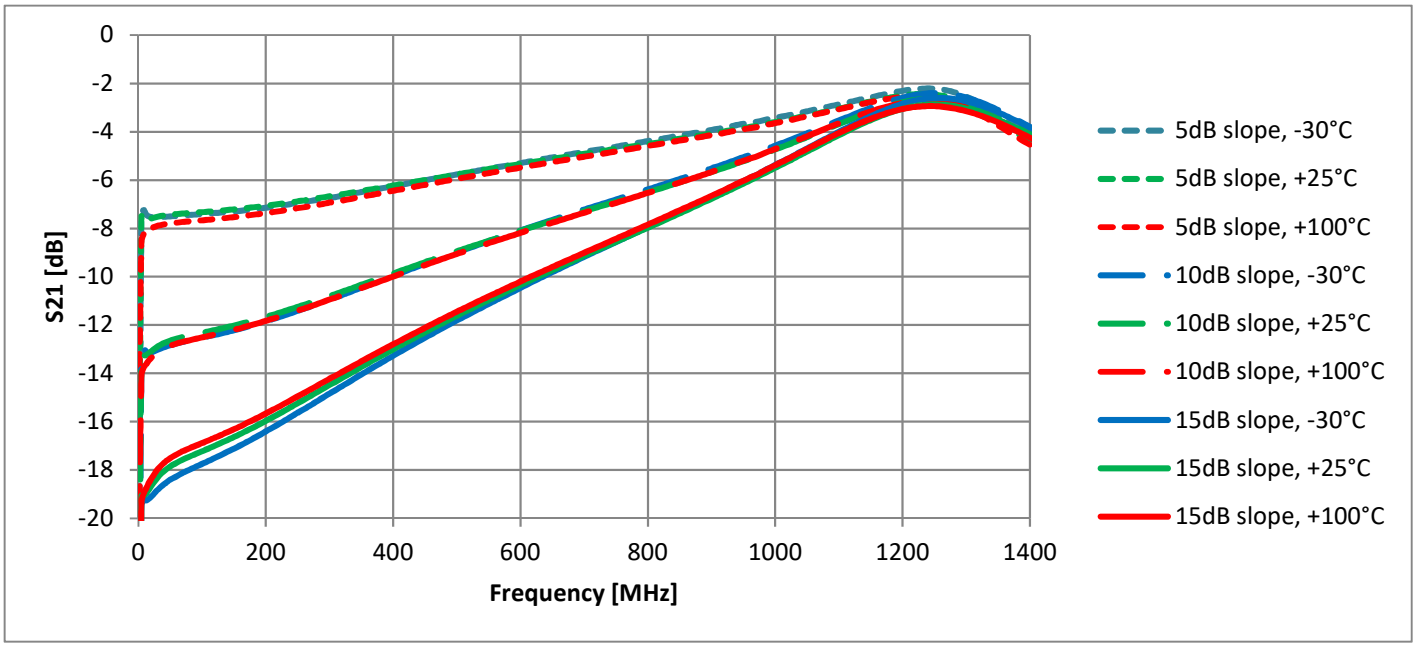
Parameter	Conditions (Vdd=5V, T_{MB}=25°C, Z_S=Z_L=75Ω)	Min	Typ	Max	Units
Control					
Control Voltage (Vc) [3], positive slope control gradient	MODE = 0V, minimum slope at Vc = 0V	0	1 to 3	5	V
Control Voltage (Vc) [3], negative slope control gradient	MODE = 5V, minimum slope at Vc = 5V	0	2 to 4	5	V
Control Voltage 2 (Vc2) [3], positive slope control gradient	MODE = 0V, minimum slope at Vc2 = 0V	0	4 to 12	20	V
Control Voltage 2 (Vc2) [3], negative slope control gradient	MODE = 5V, minimum slope at Vc2 = 20V	0	8 to 16	20	V
MODE Pin Logic Low				0.4	V
MODE Pin Logic High		1			V

Notes:
1. Slope is defined as the difference between the gain at the start frequency and the gain at the stop frequency.
2. Flatness is defined as sum of positive and negative deviation from a straight line between gain at start frequency and gain at stop frequency.
3. Either Vc or Vc2 can be used to set slope, internal 1:4 voltage divider between Vc and Vc2.

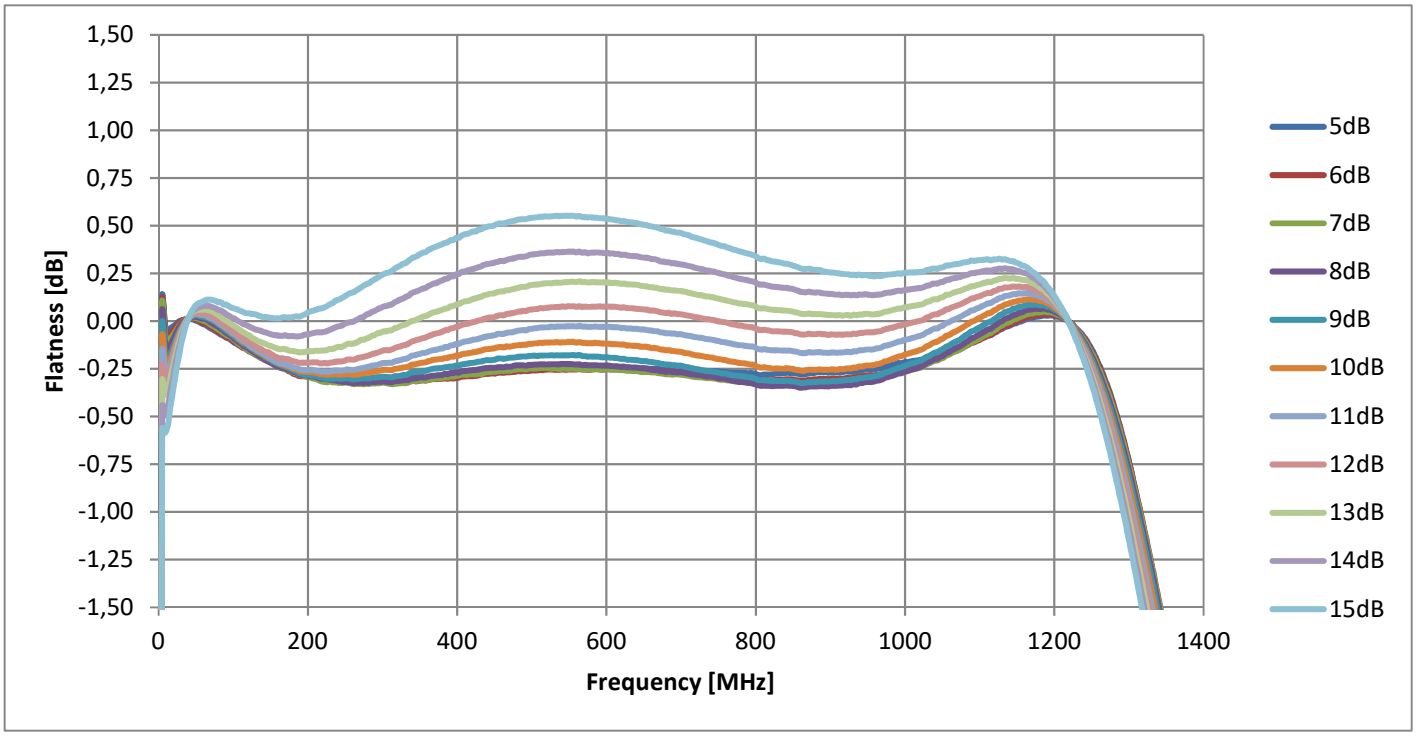
QPC7336 Slope vs. Frequency, typical



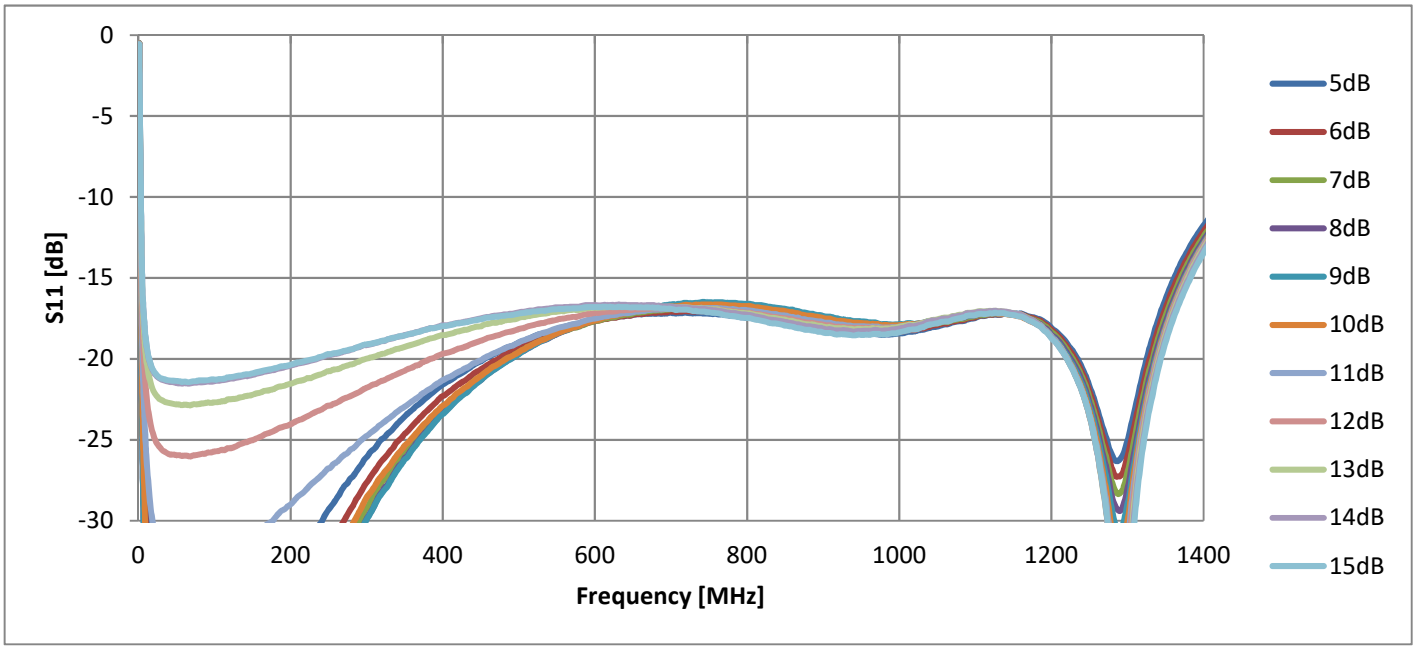
QPC7336 Slope vs. Temperature, typical



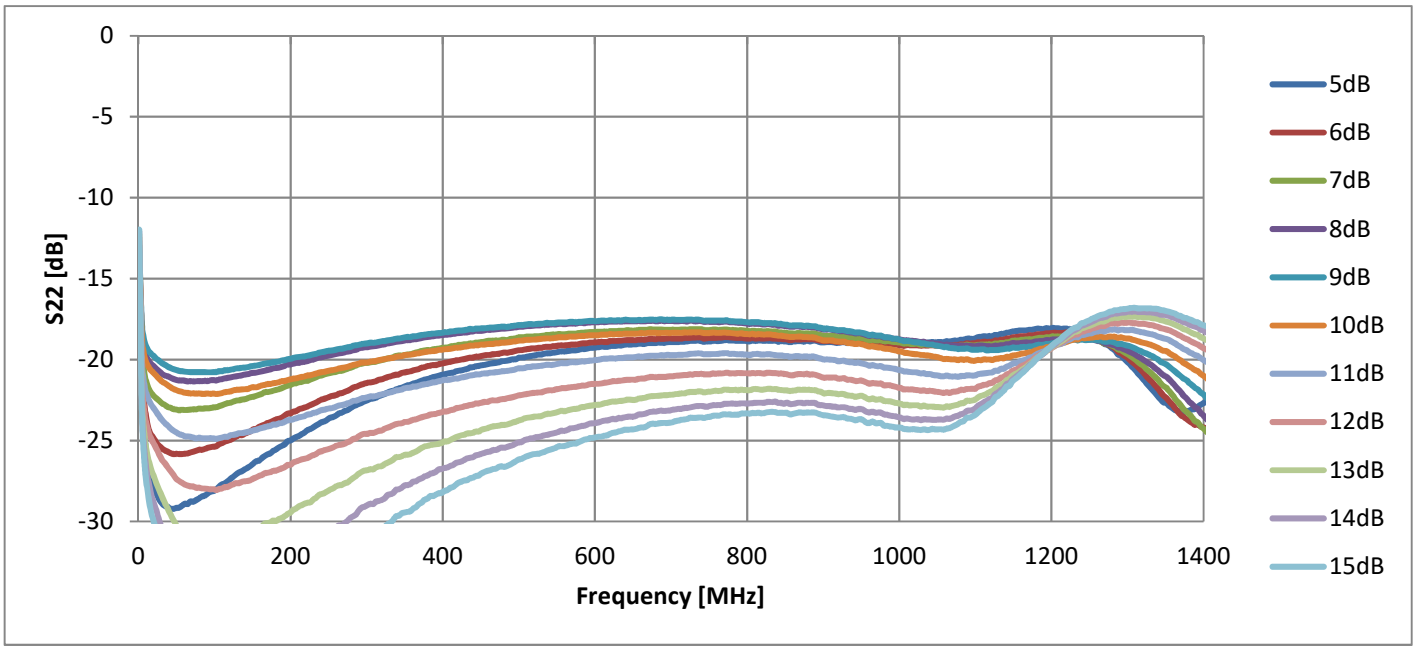
QPC7336 Flatness vs. Slope, typical



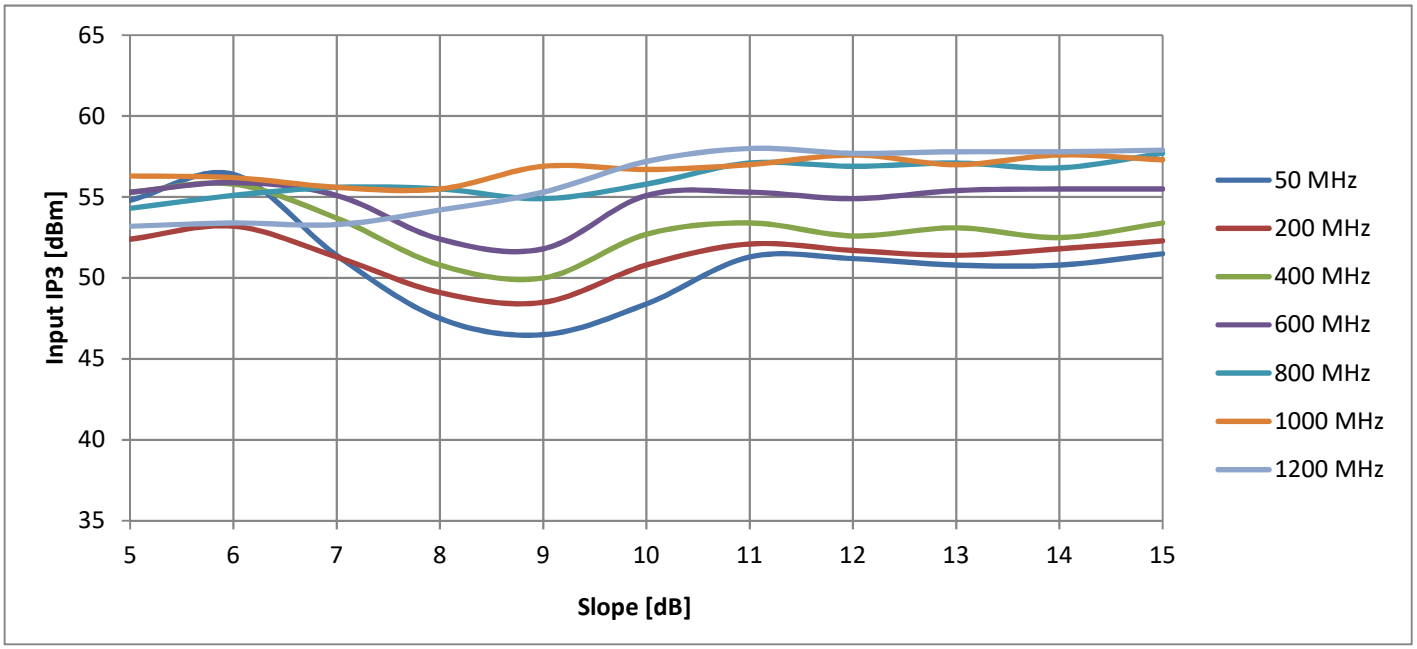
QPC7336 S11 vs. Slope, typical



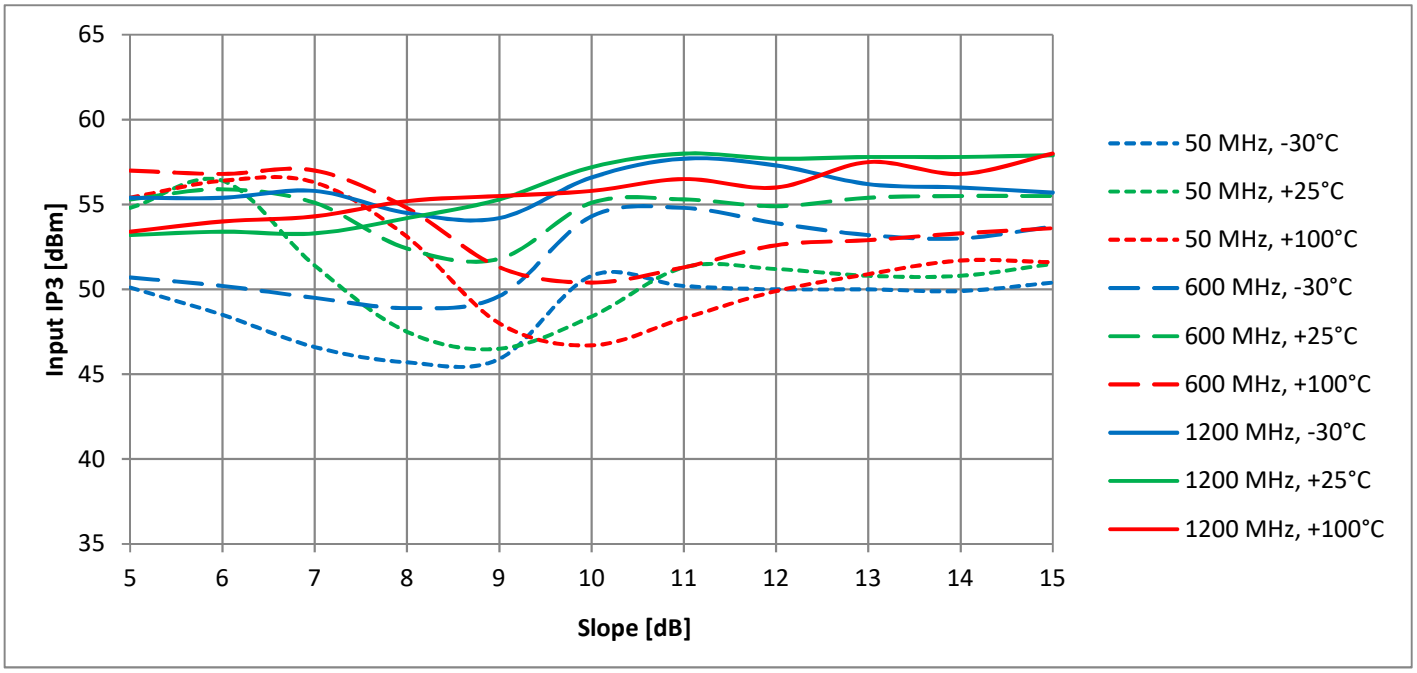
QPC7336 S22 vs. Slope, typical



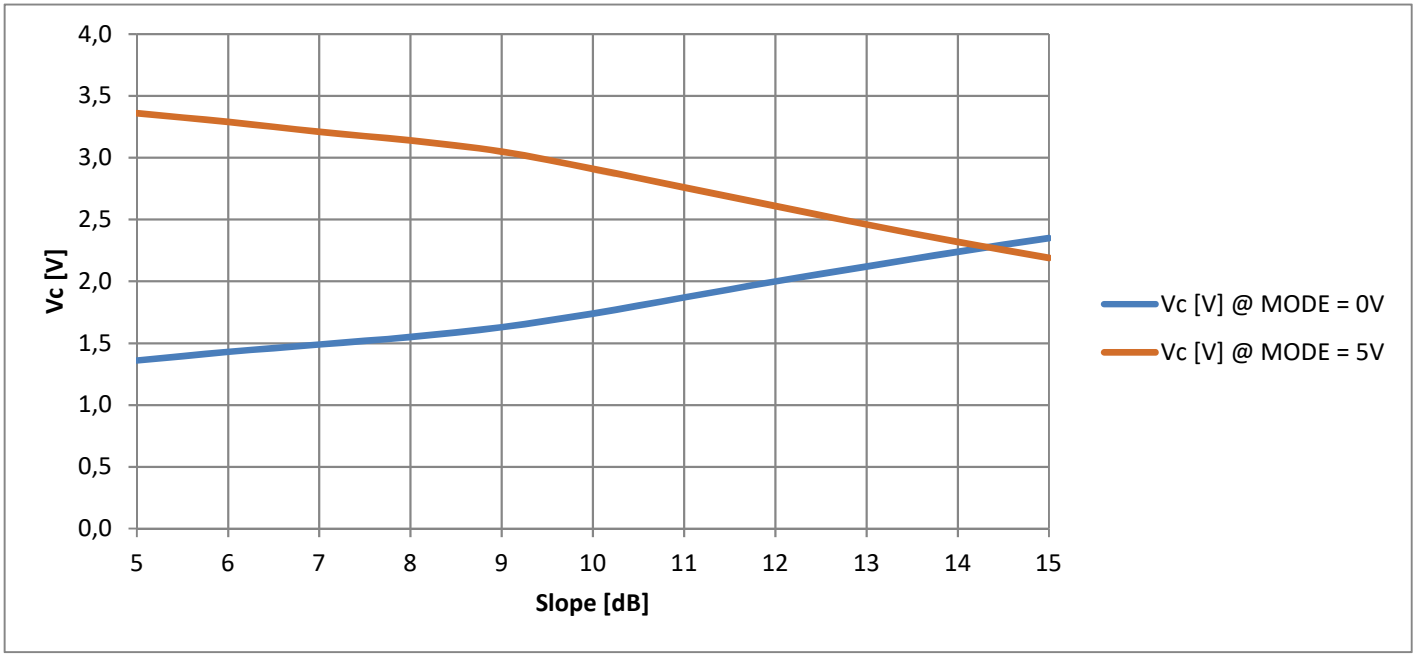
QPC7336 Input IP3 vs. Slope, typical



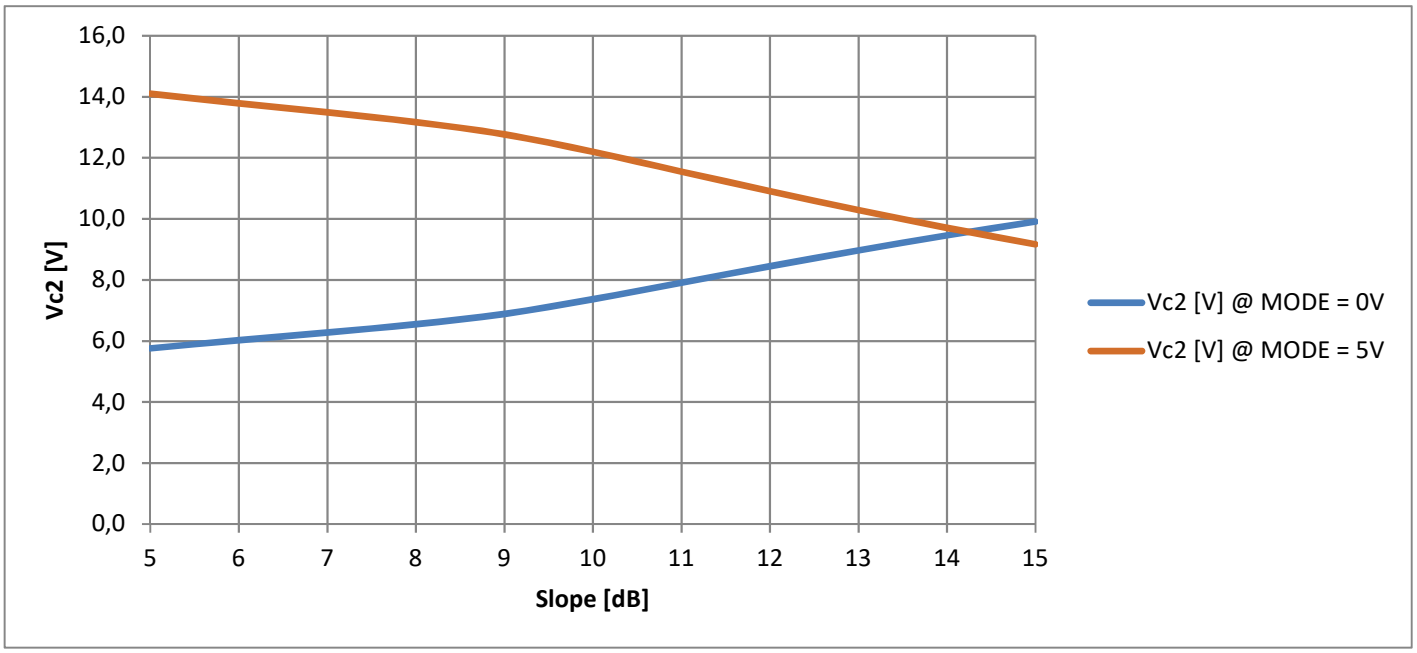
QPC7336 Input IP3 vs. Temperature, typical



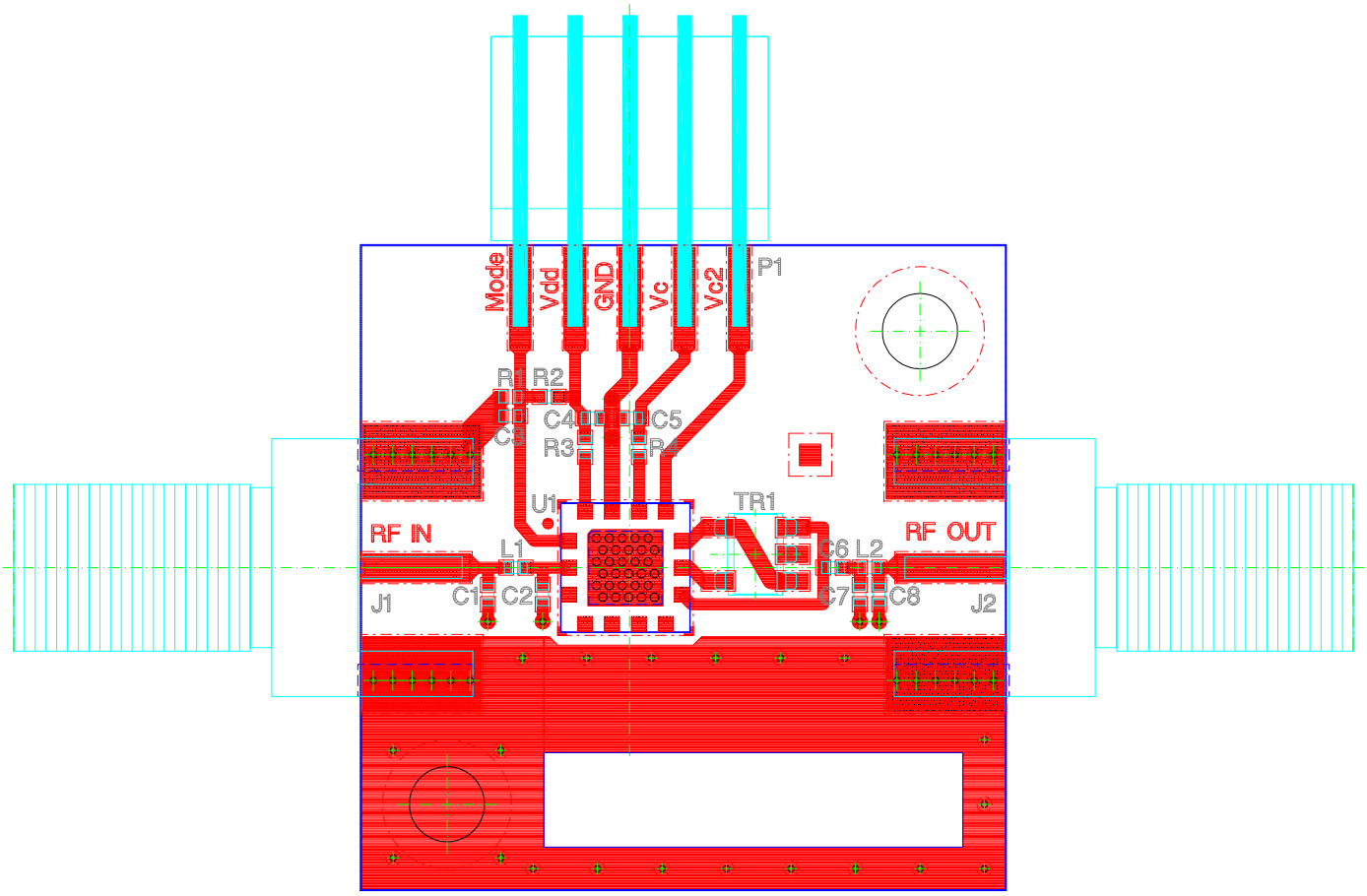
QPC7336 Slope vs. Vc, typical



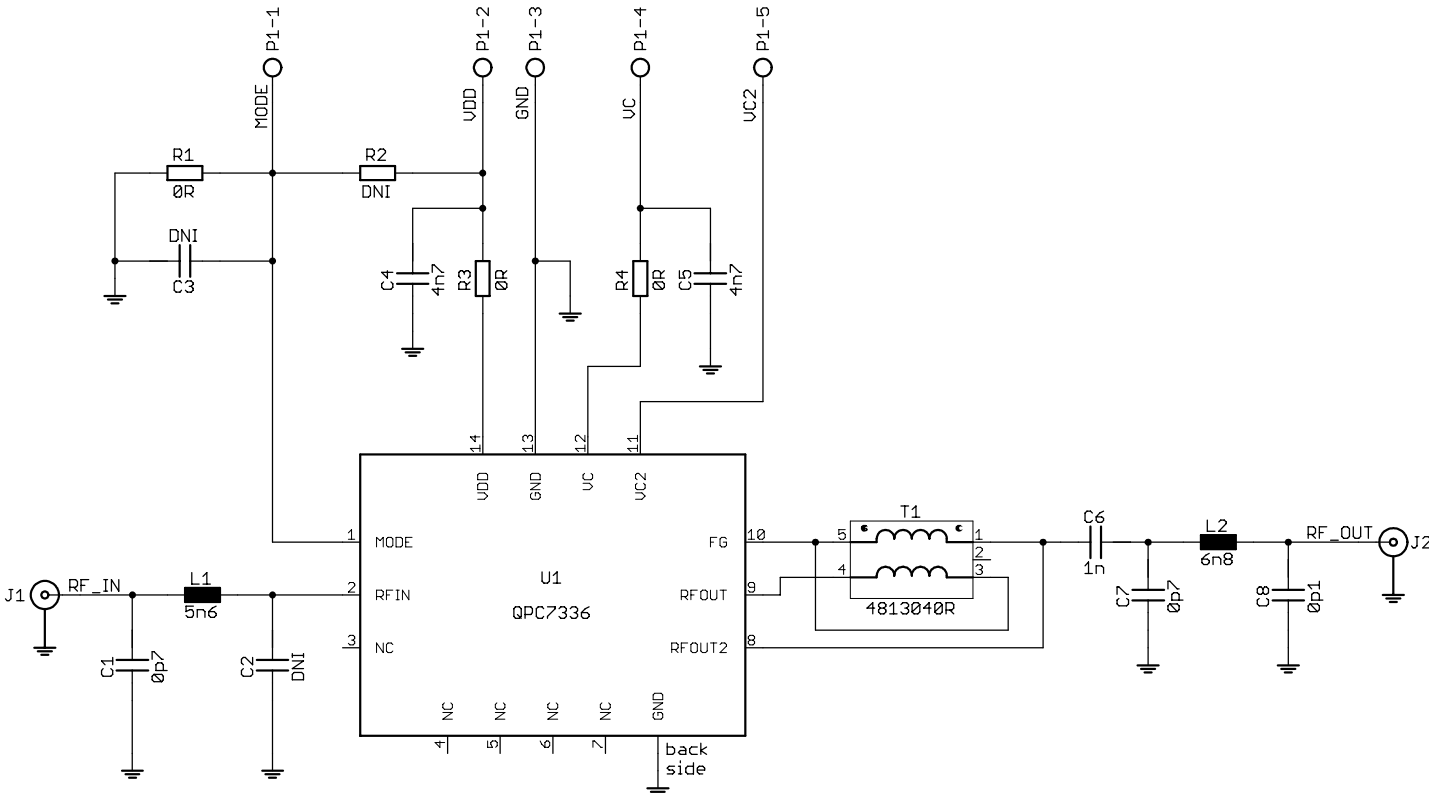
QPC7336 Slope vs. Vc2, typical



Evaluation Board Assembly Drawing



Evaluation Board Schematic



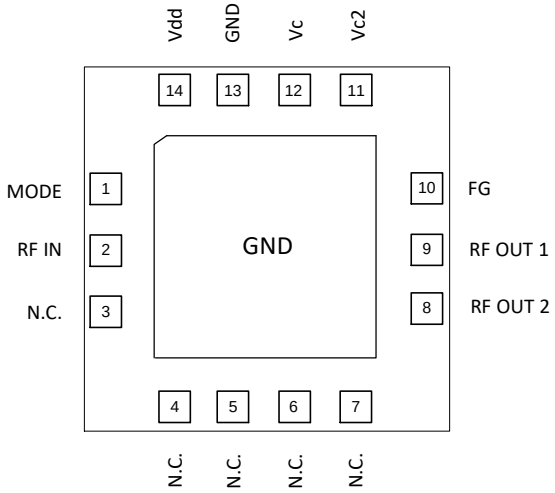
Evaluation Board Bill of Materials (BOM)

Ref. Designator	Value, package	Description	Manufacturer	Part Number
R1, R3, R4	0R, 0402	Jumper 0R	various	
C1, C7	0.7pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C4, C5	4.7nF, X7R, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C6	1nF, X7R, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C8	0.1pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
L1	5.6nH, 0402	Chip inductor	TAIYO YUDEN	HK 1005 5N6S
L2	6.8nH, 0402	Chip inductor	TAIYO YUDEN	HK 1005 6N8J
T1		Transformer	Minntronix	4813040R
J1, J2		Connector F-type, female	Amphenol	222181
P1		Connector, 2.54mm pin spacing, optional	various	
U1		Variable equalizer	QORVO	QPC7336
R2, C2, C3	DNI			

Notes: Evaluation circuit connects MODE to GND via 0R resistor (standard operation mode, increasing slope with increasing control voltage)
C1, C8 can be optimized in target application circuit for S11 and S22

Pin Configuration

Top view

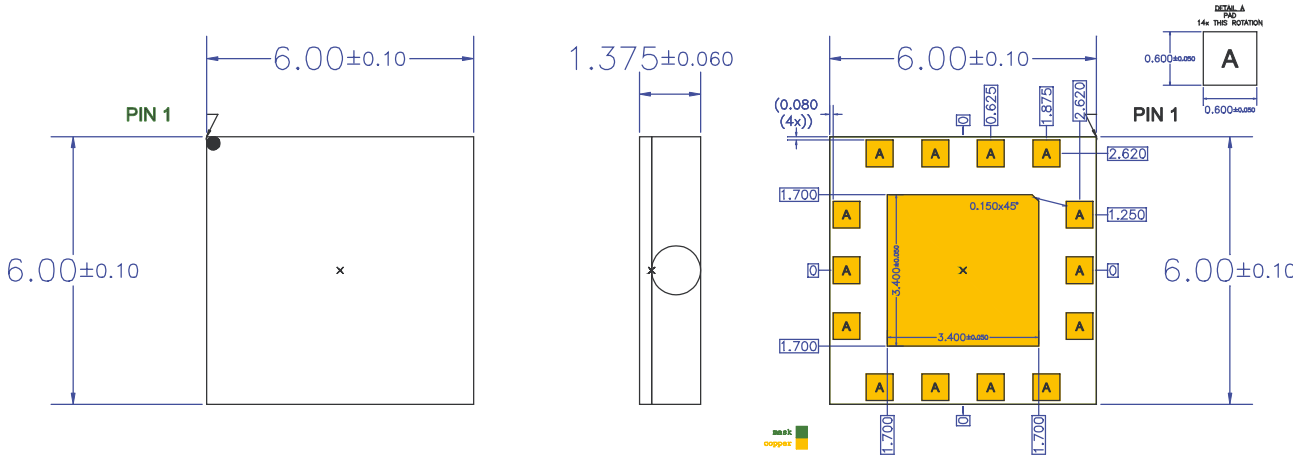


Pin Description

Pin No.	Label	Description
1	MODE	Slope control gradient (0V: positive slope control gradient or 5V: negative slope control gradient)
2	RF IN	RF input signal, AC coupled
8	RF OUT 2	Connection to balun and circuit output
9	RF OUT 1	Connection to balun
10	FG	Floating ground, connection to balun
11	Vc2	Control voltage 2
12	Vc	Control voltage
13, GND	GND	Ground
14	Vdd	+5V supply voltage
3, 4, 5, 6, 7	N.C.	Not connected

Notes: Either Pin11 or Pin12 can be used to set slope, internal 1:4 voltage divider between Pin11 and Pin12

Package Outline Drawing (Dimensions in millimeters)



TOP VIEW

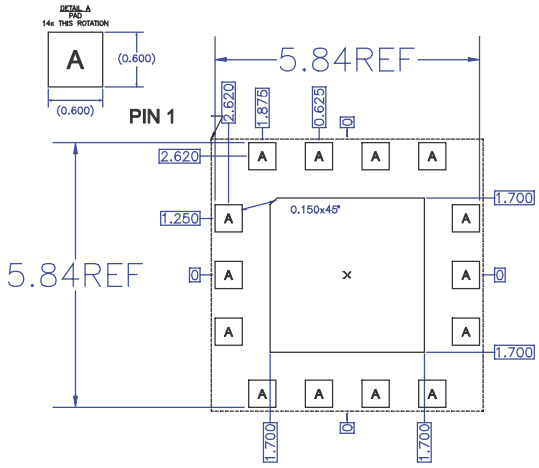
SIDE VIEW

BOTTOM VIEW

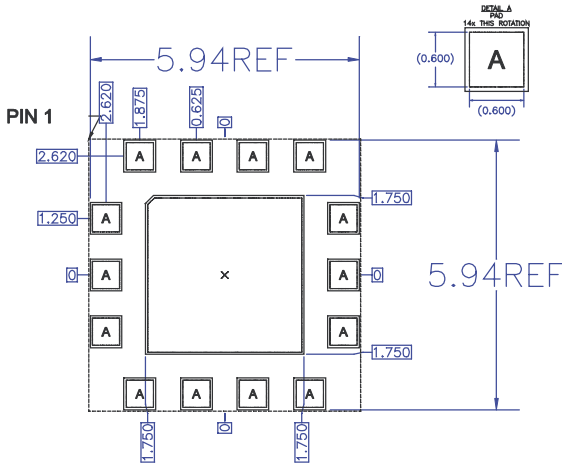
Notes:

1. Dimension and tolerance formats conform to ASME Y14.5M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
4. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Metal Land Pattern (Dimensions in millimeters)



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 2 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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