PE43650

Document Category: Preliminary Specification

50 Ω RF Digital Attenuator 5-bit, 15.5 dB, 9 kHz - 6 GHz

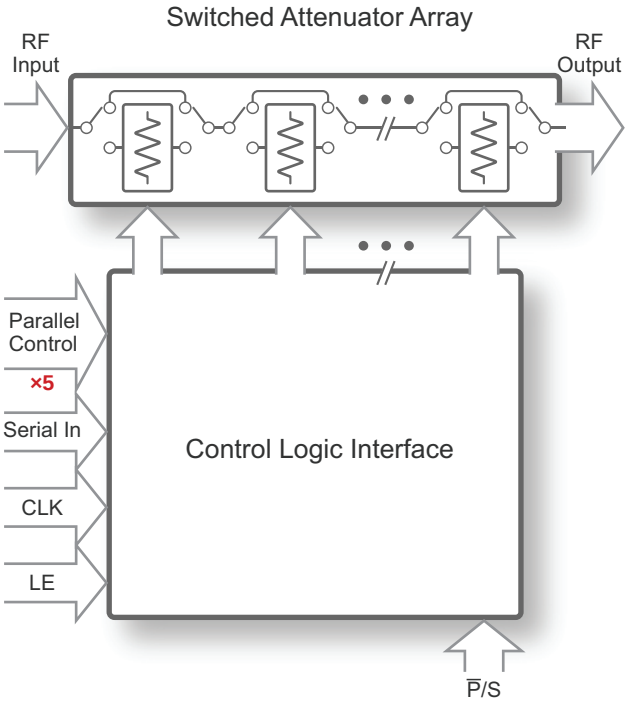
Features

- Attenuation: 0.5 dB steps to 15.5 dB
- High linearity: Typical +58 dBm IP3
- Excellent low-frequency performance
- Programming modes:
  - Direct parallel
  - Latched parallel
  - Serial
- CMOS-compatible
- No DC blocking capacitors required
- Packaged in a 24-lead 4x4x0.85 mm QFN

Applications

- 3G / 4G wireless infrastructure
  - RF/IF gain control
  - Base stations (BTS) and remote radio heads (RRH)
  - Optical and RF repeaters
  - Distributed antenna system (DAS)
- Land mobile radio system
- Point-to-point communication system

Figure 1 • *PE43650 Functional Diagram*



Product Description

The PE43650 is a high linearity, 5-bit RF Digital Step Attenuator (DSA). This highly versatile DSA covers a 15.5 dB attenuation range in 0.5 dB steps. The Peregrine 50Ω RF DSA provides multiple CMOS control interfaces. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and low power consumption. Performance does not change with VDD due to on-board regulator. This Peregrine DSA is available in a 4x4 mm 24-lead QFN footprint.

The PE43650 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

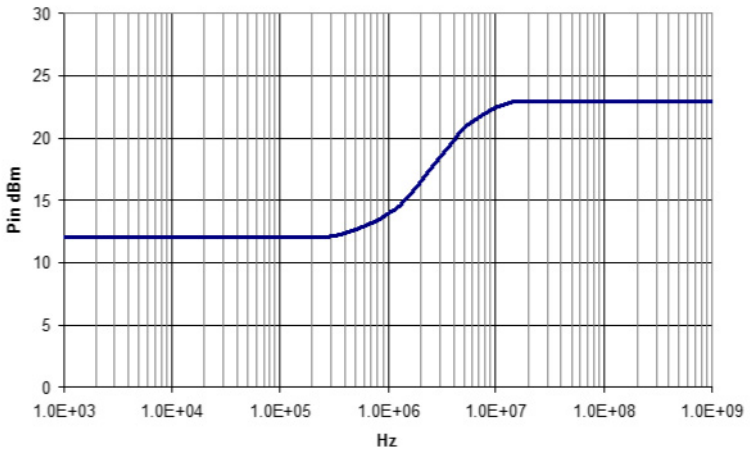
Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE43650*

Parameter/Condition	Min	Max	Unit
Power supply voltage (V_{DD})	-0.3	6.0	V
Voltage on any Digital input (V_I)	-0.3	5.8	V
Storage temperature range (T_{ST})	-65	150	°C
Input power (50Ω) (P_{IN}) 9 kHz ≤ 20 MHz 20 MHz ≤ 6 GHz		 Fig. 2 +23	 dBm dBm
ESD voltage (HBM)(*) ESD voltage (machine model)		500 100	V V
Note: * Human Body Model (HBM, MIL_STD 883 Method 3015.7)			

Figure 2 • *Maximum Power Handling Capability*



Recommended Operating Conditions

Table 2 lists the recommending operating conditions for the PE43650. Devices should not be operated outside the operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE43650*

Parameter	Min	Typ	Max	Unit
V_{DD} Power Supply Voltage	3.0	3.3		V
V_{DD} Power Supply Voltage		5.0	5.5	V
I_{DD} Power Supply Current		70	350	µA
Digital Input High	2.6		5.5	V
P_{IN} Input power (50Ω): 9 kHz ≤ 20 MHz 20 MHz ≤ 6 GHz			 **Fig. 2** +23	 dBm dBm
T_{OP} Operating temperature range	-40	25	85	°C
Digital Input Low	0		1	V
Digital Input Leakage[1]			15	µA

Note: * 1. Input leakage current per Control pin.

Electrical Specifications

Table 3 provides the PE43650 key electrical specifications @ +25°C, V_{DD} = 3.3 V or 5.0 V, unless otherwise specified.

Table 3 • *PE43650 Electrical Specifications*

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Frequency Range			9 kHz		6 GHz	
Attenuation Range	0.5 dB Step			0 – 15.5		dB
Insertion Loss		9 kHz ≤ 6 GHz		2.4	2.9	dB
Attenuation Error	0 dB - 15.5 dB Attenuation settings 0 dB - 7.5 dB Attenuation settings 8 dB - 15.5 dB Attenuation settings 0 dB - 15.5 dB Attenuation settings	9 kHz < 4 GHz 4 GHz ≤ 6 GHz 4 GHz ≤ 6 GHz 4 GHz ≤ 6 GHz			±(0.3 + 3%) +0.4 + 4% +0.6 + 8% -0.2 - 3%	dB dB dB dB
Return Loss		9 kHz - 6 GHz		17		dB
Relative Phase	All States	9 kHz - 6 GHz		18		deg
P1dB (note 1)	Input	20 MHz - 6 GHz	30	32		dBm
IIP3	Two tones at +18 dBm, 20 MHz spacing	20 MHz - 6 GHz		58		dBm
Typical Spurious Value		1 MHz		-110		dBm
Video Feed Through				10		mVpp
Switching Time	50% DC CTRL to 10% / 90% RF			650		ns
RF Trise/Tfall	10% / 90% RF			400		ns
Settling Time	RF settled to within 0.05 dB of final value RBW = 5 MHz, Averaging ON.			4		µs

Note: 1. Please note Maximum Operating Pin (50Ω) of +23dBm as shown in **Table 2**.

Switching Frequency

The PE43650 has a maximum 25 kHz switching frequency.

Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Control Voltage

Table 4 provides the control voltage table for the PE43650.

Table 4 • *Control Voltage for PE43650*

State	Bias Condition
Low	0 to +1.0 Vdc at 2 µA (typ)
High	+2.6 to +5 Vdc at 10 µA (typ)

Latch and Clock Specifications

Table 5 provides the latch and clock specifications for the PE43650.

Table 5 • *Latch and Clock Specifications*

Latch Enable	Shift Clock	Function
X	↑	Shift Register Clocked
↑	X	Contents of shift register transferred to attenuator core

Truth Tables

Table 6 and Table 7 provide the truth tables for the PE43650.

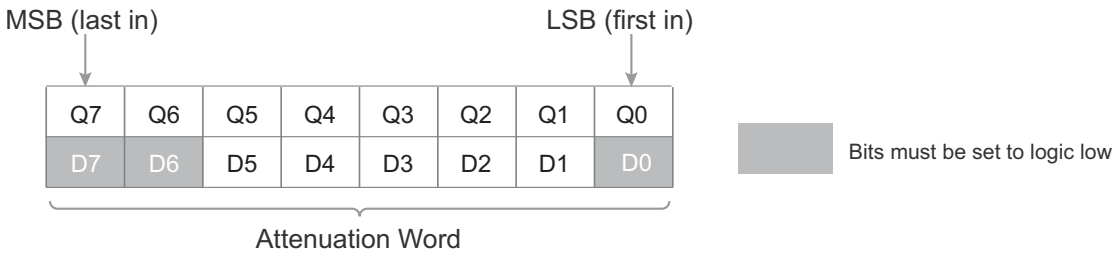
Table 6 • *Parallel Truth Table*

Parallel Control Setting					Attenuation Setting RF1-RF2
D5	D4	D3	D2	D1	
L	L	L	L	L	Reference I.L.
L	L	L	L	H	0.5 dB
L	L	L	H	L	1 dB
L	L	H	L	L	2 dB
L	H	L	L	L	4 dB
H	L	L	L	L	8 dB
H	H	H	H	H	15.5 dB

Table 7 • *Attenuation Word Truth Table*

Attenuation Word								Attenuation Setting RF1-RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	L	H	H	H	H	H	L	15.5 dB

Figure 3 • *Serial Register Map*



The Attenuation Word is derived directly from the attenuation value.

For example, to program the 12.5 dB state:

Attenuation Word: Multiply by 4 and convert to binary → 4 * 12.5 dB → 50 → 00110010
Serial Input: 00110010

Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE43650. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S=LOW selecting the parallel interface and $\overline{P}$/S=HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of five CMOS-compatible control lines that select the desired attenuation state, as shown in **Table 6**.

The parallel interface timing requirements are defined by **Figure 5** (Parallel Interface Timing Diagram), **Table 9** (Parallel Interface AC Characteristics), and switching speed (**Table 3**).

For *latched*-parallel programming the latch enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (*per* **Figure 5**) to latch new attenuation state into device.

For *direct* parallel programming, the latch enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial Interface

The serial interface is a 8-bit serial-in, parallel-out shift register buffered by a transparent latch. The 8-bits make up the attenuation word that controls the DSA. **Figure 4** illustrates a example timing diagram for programming a state.

The serial-interface is controlled using three CMOS-compatible signals: Serial-in (SI), clock (CLK), and latch enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The attenuation word truth table is listed in **Table 7**. A programming example of the serial register is illustrated in **Table 3**. The serial timing diagram is illustrated in **Figure 3**. It is required that all parallel pins be grounded when the DSA is used in serial mode.

Power-up Control Settings

The PE43650 will always initialize to the maximum attenuation setting (15.5 dB) on power-up for both the serial and latched-parallel modes of operation and will remain in this setting until the user latches in the next programming word. In direct-parallel mode, the DSA can be preset to any state within the 15.5 dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400-µs delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (15.5 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Dynamic operation between serial and parallel programming modes is possible.

If the DSA powers up in serial mode ($\overline{P}$/S = HIGH), all the parallel control inputs DI[5:1] must be set to logic low. Prior to toggling to parallel mode, the DSA must be programmed serially to ensure D[7] is set to logic low.

If the DSA powers up in either latched or direct-parallel mode, all parallel pins DI[5:1] must be set to logic low prior to toggling to serial mode ($\overline{P}$/S = HIGH), and held low until the DSA has been programmed serially to ensure bit D[7] is set to logic low.

The sequencing is only required power-once on power-up. Once completed, the DSA may be toggled between serial and parallel programming modes at will.

Timing Diagrams

Figure 4 provides the serial programming register map for the PE43650.

Figure 4 • *Serial Timing Diagram*

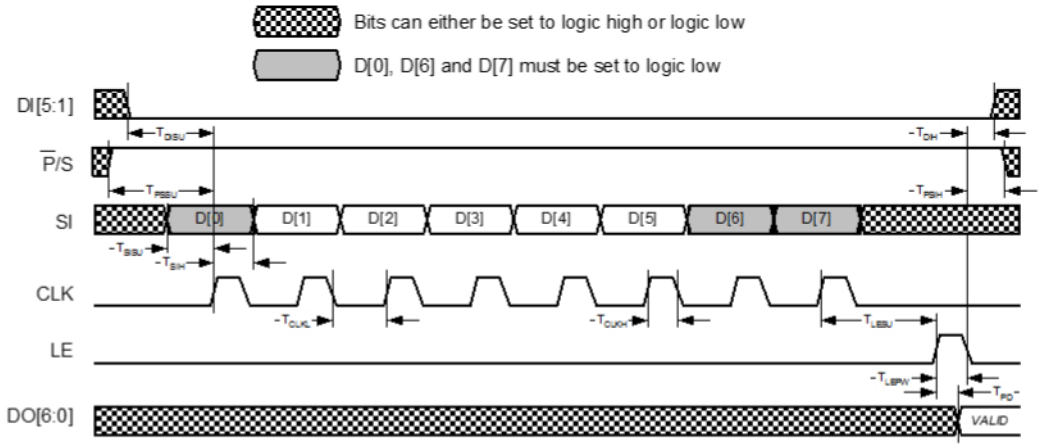


Figure 5 • *Latched-Parallel/Direct Parallel Timing Diagram*

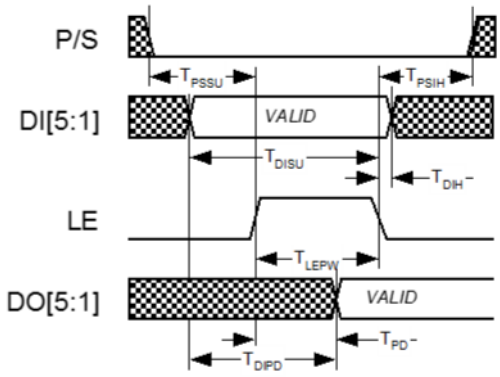


Table 8 • *Serial Interface AC Characteristics*

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial data clock frequency	-	10	MHz
T_{CLKH}	Serial clock HIGH time	30	-	ns
T_{CLKL}	Serial clock LOW time	30	-	ns
T_{LESU}	Last serial clock rising edge setup time to Latch Enable rising edge	10	-	ns
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{SISU}	Serial data setup time	10	-	ns
T_{SIH}	Serial data hold time	10	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{ASU}	Address setup time	100	-	ns
T_{AH}	Address hold time	100	-	ns
T_{PSSU}	Parallel/serial setup time	100	-	ns
T_{PSH}	Parallel/serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns

Notes:
V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +85 °C, unless otherwise specified.

Table 9 • *Parallel and Direct Interface AC Characteristics*

Symbol	Parameter	Min	Max	Unit
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{PSSU}	Parallel/serial setup time	100	-	ns
T_{PSH}	Parallel/serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns
T_{DIPD}	Digital register delay (internal, direct mode only)	-	5	ns

Notes:
V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +85 °C, unless otherwise specified.

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE43650 digital step attenuator.

Direct Parallel Programming Procedure

For automated direct-parallel programming, connect the test harness provided with the EVK from the parallel port of the PC to the J1 and serial header pin and set the D0-D6 SP3T switches to the 'MIDDLE' toggle position. Position the parallel/serial ($\overline{P}$/S) select switch to the parallel (or left) position. The evaluation software is written to operate the DSA in either parallel or serial-addressable mode. Ensure that the software is set to program in direct-parallel mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

For manual direct-parallel programming, disconnect the test harness provided with the EVK from the J1 and serial header pins. Position the parallel/serial ($\overline{P}$/S) select switch to the parallel (or left) position. The LE pin on the serial header must be tied to VDD. Switches D0-D6 are SP3T switches which enable the user to manually program the parallel bits. When any input D0-D6 is toggled 'UP', logic high is presented to the parallel input. When toggled 'DOWN', logic low is presented to the parallel input. Setting D0-D6 to the 'MIDDLE' toggle position presents an OPEN, which forces an on-chip logic low. **Table 6** depicts the parallel programming truth table and **Figure 5** illustrates the parallel programming timing diagram.

Latched Parallel Programming Procedure

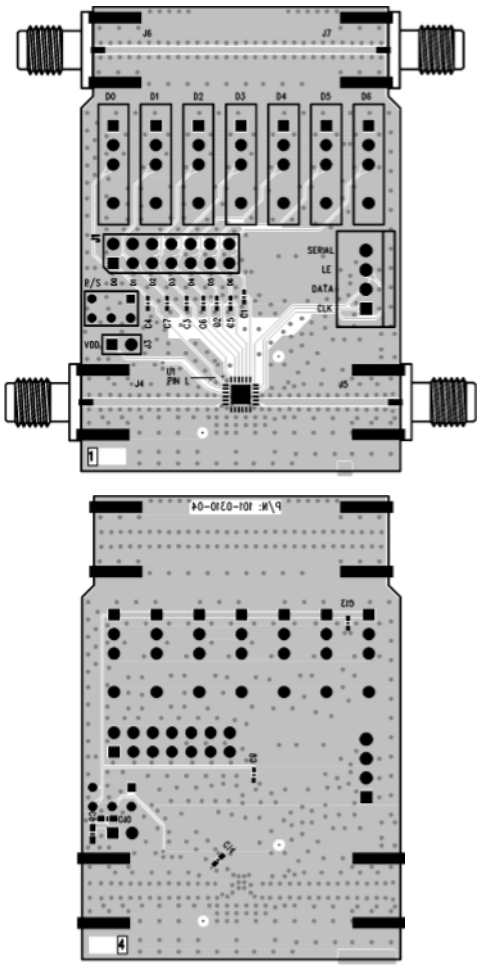
For automated latched-parallel programming, the procedure is identical to the direct-parallel method.The user only must ensure that Latched-parallel is selected in the software.

For manual latched-parallel programming, the procedure is identical to direct-parallel except now the LE pin on the serial header must be logic low as the parallel bits are applied. The user must then pulse LE from 0V to VDD and back to 0V to latch the programming word into the DSA. LE must be logic low prior to programming the next word.

Serial Programming Procedure

Position the parallel/serial ($\overline{P}$/S) select switch to the serial (or right) position. The evaluation software is written to operate the DSA in either parallel or serial mode. Ensure that the software is set to program in serial mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

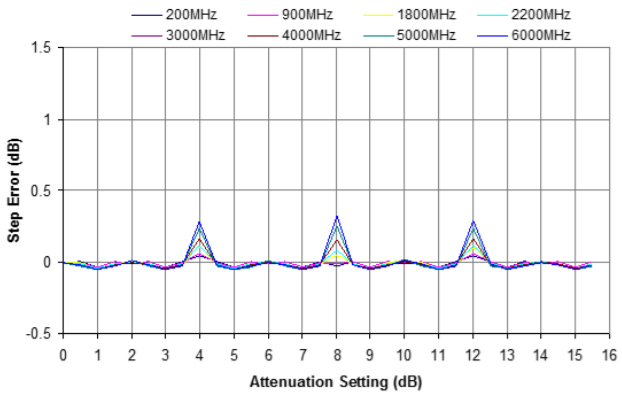
Figure 6 • *Evaluation Board Layout for PE43650*



Typical Performance Data

Figure 7–Figure 16 show the typical performance data at T = +25C, unless otherwise specified.

Figure 7 • *0.5 dB Step Error vs. Frequency**



*Monotonicity is held so long as Step-Error does not cross below -0.5.

Figure 8 • *1 dB Attenuation vs. Attenuation State*

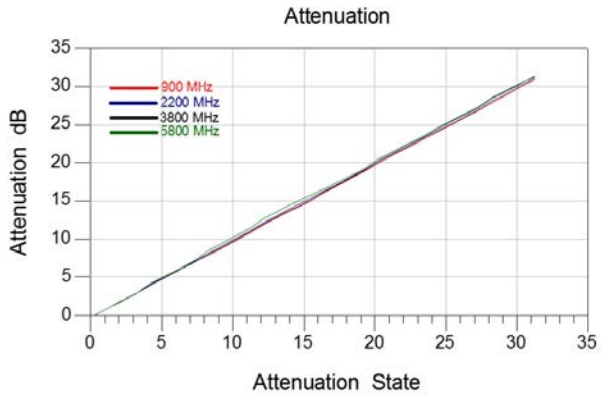


Figure 9 • *0.5 dB Major State Bit Error*

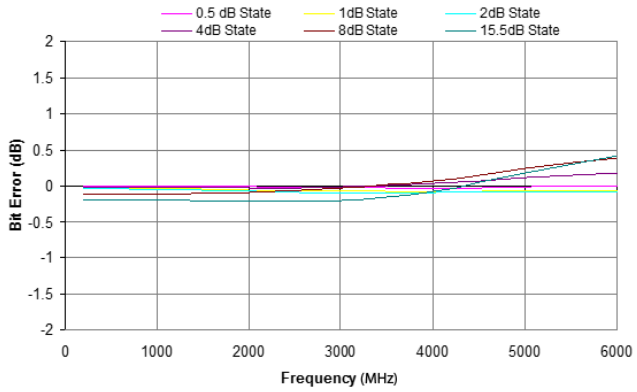


Figure 10 • *0.5 dB Attenuation Error vs. Frequency*

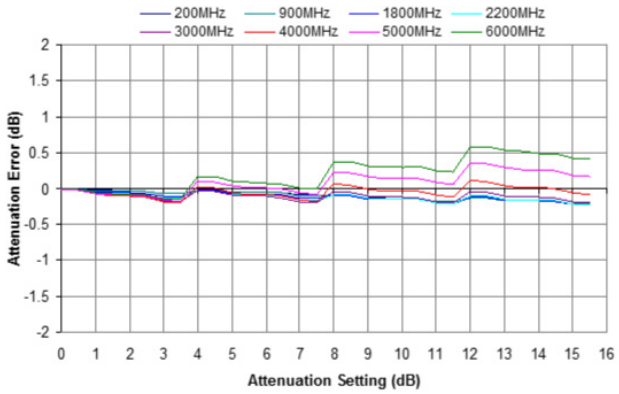


Figure 11 • *Insertion Loss vs. Temperature*

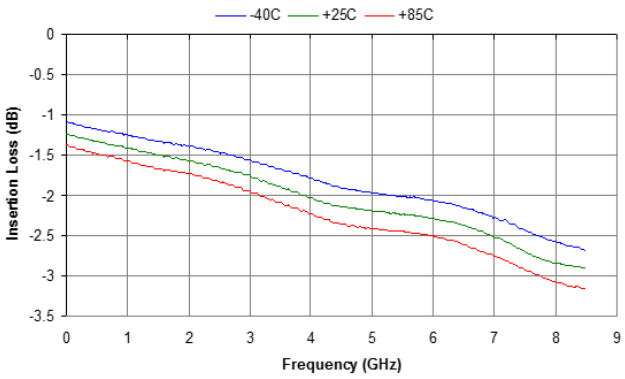


Figure 12 • *Input Return Loss vs. Attenuation @ T = +25C*

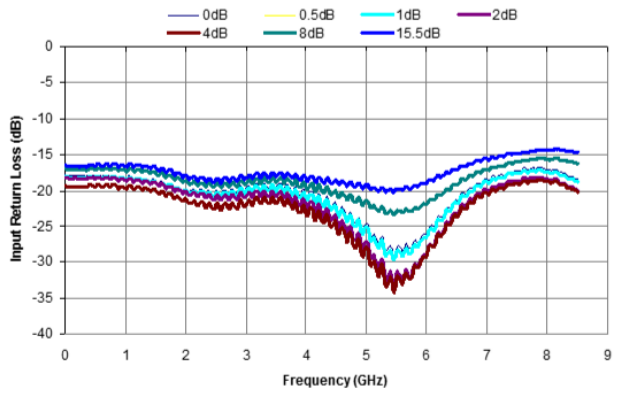


Figure 13 • *Output Return Loss vs. Attenuation @ T = +25C*

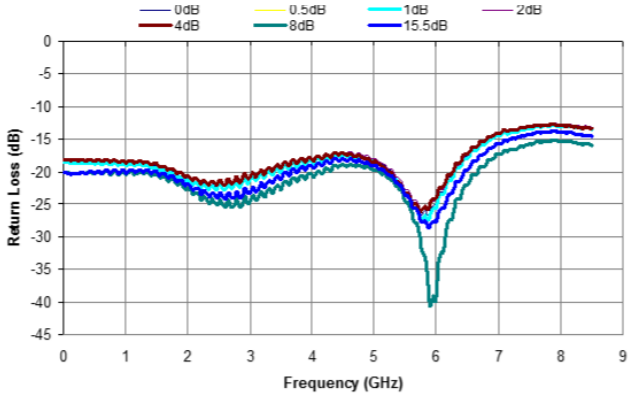


Figure 14 • *Relative Phase vs. Frequency*

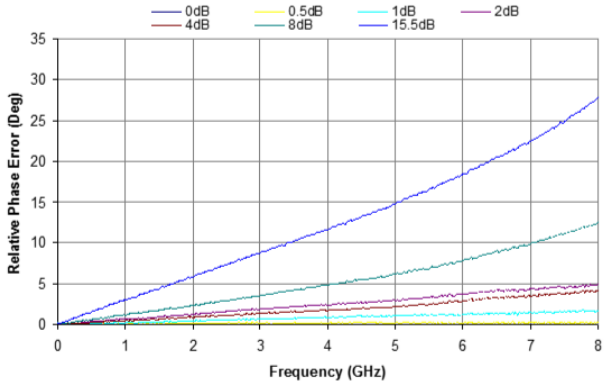


Figure 15 • *Attenuation Error vs. Temperature @ 6 GHz*

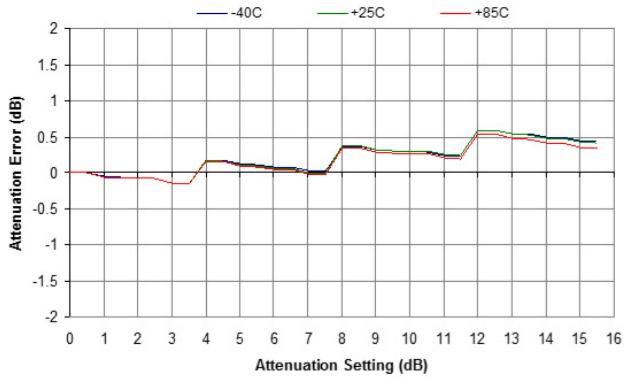
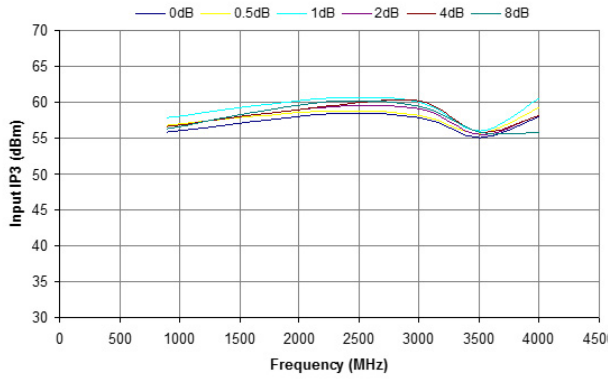


Figure 16 • *Input IP3 vs. Frequency*



Pin Information

This section provides pinout information for the PE43650. **Figure 17** shows the pin map of this device for the available package. **Table 10** provides a description for each pin.

Figure 17 • *Pin Configuration (Top View)*

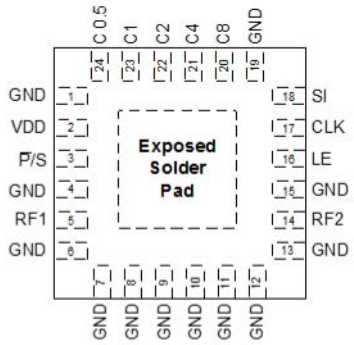


Table 10 • *Pin Descriptions for PE43650*

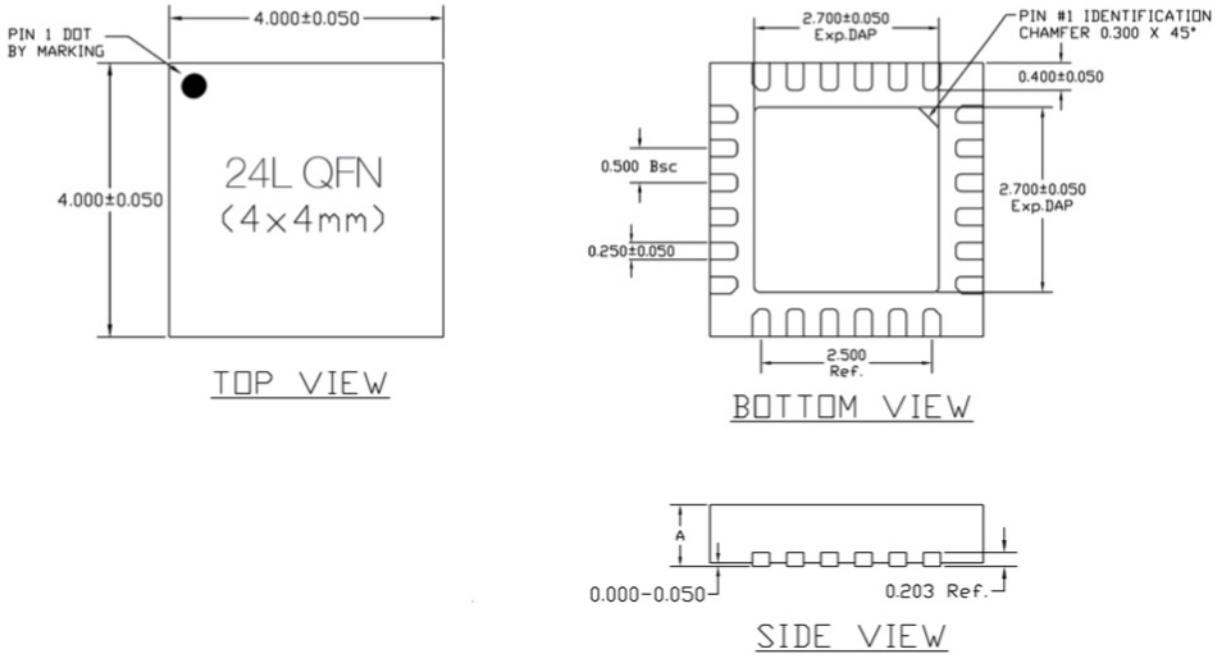
Pin No.	Pin Name	Description
1	GND	Ground
2	V_{DD}	Power supply pin
3	$\overline{P}$/S	Parallel/serial mode select
4	GND	Ground
5	RF1	RF1 port
6 - 13	GND	Ground
14	RF2	RF2 port
15	GND	Ground
16	LE	Serial interface latch enable input
17	CLK	Serial interface clock input
18	SI	Serial interface data input
19	GND	Ground
20	C8 (D5)	Parallel control bit, 8 dB
21	C4 (D4)	Parallel control bit, 4 dB
22	C2 (D3)	Parallel control bit, 2 dB
23	C1 (D2)	Parallel control bit, 1 dB
24	C0.5 (D1)	Parallel control bit, 0.5 dB
Paddle	GND	Ground for proper operation
Note: Ground C0.5, C1 C2, C4, C8, if not in use.		

Packaging Information

This section provides packaging data including the package drawing, package marking and tape-and-reel information.

Package Drawing

Figure 18 • *Package Drawing*



Top-Marking Specification

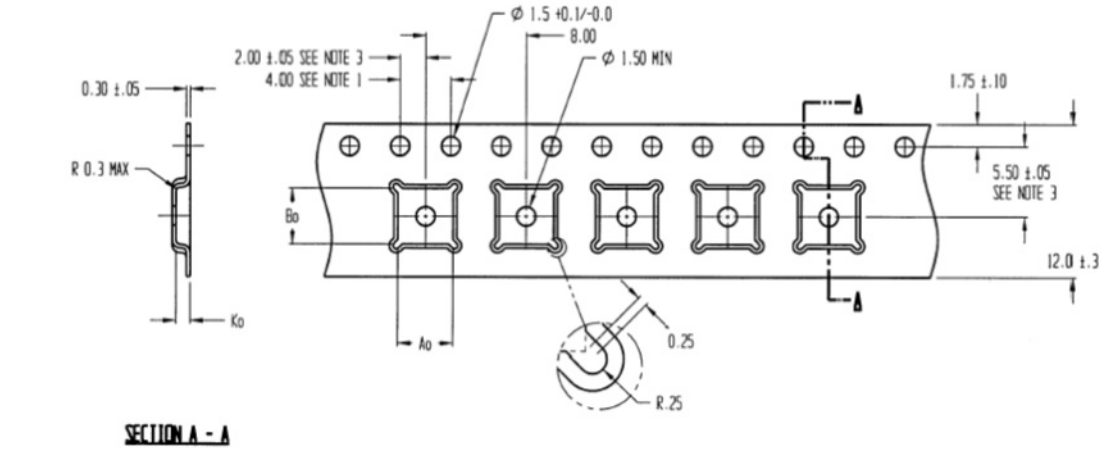
Figure 19 • *Marking Specifications*



● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Last six digits of lot number

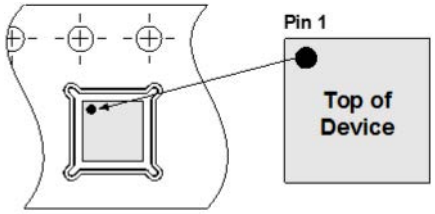
Tape and Reel Specification

Figure 20 • *Tape and Reel Drawing*



Ao = 4.35
Bo = 4.35
Ko = 1.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE



Device Orientation in Tape

Ordering Information

Table 11 lists the available ordering codes for the PE43650 as well as available shipping methods.

Table 11 • *Order Codes for PE43650*

Order Codes	Description	Packaging	Shipping Method
PE43650A-Z	PE43650 Digital Step Attenuator	Green 24-lead 4x4mm QFN	3000 units / T&R
EK43650-01	PE43650 Evaluation Kit	Evaluation Kit	1 / Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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