# PE43665

## Preliminary Specification

*UltraCMOS® RF Digital Step Attenuator, 1 MHz–2 GHz*

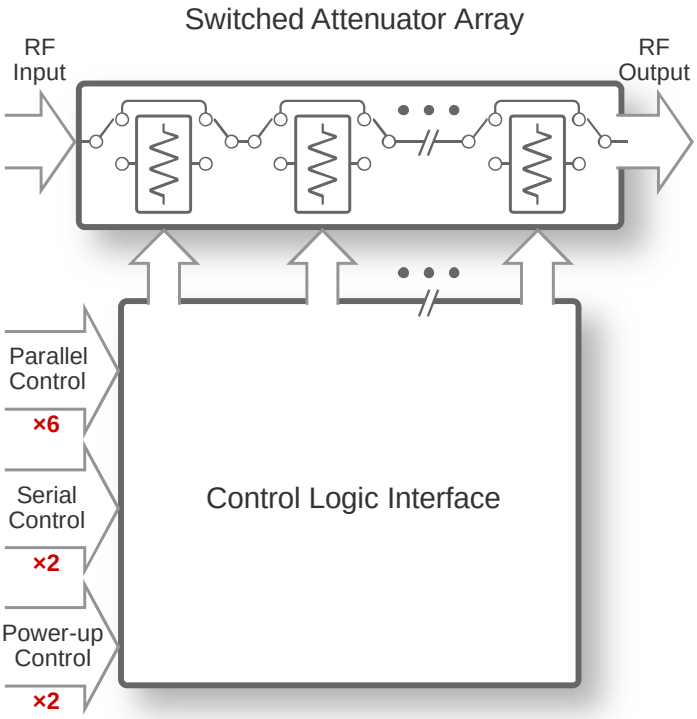
## Features

- 75Ω impedance
- Attenuation: 0.5 dB steps to 31.5 dB
- Low distortion for CATV and multi-carrier applications
- Flexible parallel and serial programming interfaces
- Unique power-up state selection
- Positive CMOS control logic
- High attenuation accuracy and linearity over temperature and frequency
- Very low power consumption
- Single-supply operation
- Packaged in a 20 lead 4x4 mm QFN

## Applications

- DOCSIS 3.1/3.0 customer premises equipment (CPE) and infrastructure
- Satellite CPE and infrastructure
- Fiber CPE and infrastructure

**Figure 1 • *Functional Schematic Diagram***




## Product Description

The PE43665 is a 75-ohm high-linearity, 6-bit RF Digital Step Attenuator (DSA) covering a 31.5 dB attenuation range in 0.5 dB steps. The PE43665 provides both a parallel (latched or direct mode) and serial CMOS control interface, operates on a single 3-volt supply and maintains high attenuation accuracy over frequency and temperature. It also has a unique control interface that allows the user to select an initial attenuation state at power-up. The PE43665 exhibits very low insertion loss and low power consumption. This functionality is delivered in a 4x4 mm QFN footprint.

The PE43665 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

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# Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in Table 1 may cause permanent damage. Operation should be restricted to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

## ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices.

Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 1.

## Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

**Table 1 • *Absolute Maximum Ratings***

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | -0.3 | 4.0 | V |
| $V_I$ | Voltage on any input | -0.3 | $V_{DD}$+ 0.3 | V |
| $T_{ST}$ | Storage temperature range | -65 | 150 | °C |
| $P_{IN}$ | Input power (50Ω) | | +30 | dBm |
| $V_{ESD}$ | ESD voltage (Human Body Model)(1) | | 500 | V |
| 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7) | | | | |

# Recommended Operating Conditions

**Table 2 • *Recommended Operating Conditions for PE43665***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ Power Supply Voltage | 2.7 | 3.0 | 3.3 | V |
| $I_{DD}$ Power Supply Current | | | 100 | µA |
| Digital Input High | 0.7x$V_{DD}$ | | | V |
| Digital Input Low | | | 0.3x$V_{DD}$ | V |
| Digital Input Leakage | | | 1 | µA |
| Input Power | | | +24 | dBm |
| Temperature range | -40 | | 85 | °C |

## Table 3 • *Electrical Specifications @ +25 °C, $V_{DD}$ = 3.0V, $Z_o$ = 75 Ω*

| Parameter | Test Conditions | Frequency | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Operation Frequency | | | 1 | | 2000 | MHz |
| Insertion Loss[2] | | 1 MHz ≤ 1.2 GHz | - | 1.4 | 1.8 | dB |
| Attenuation Accuracy | Any bit or bit combination | 1 MHz ≤ 1.2 GHz | - | - | ±(0.15 + 4% of attenuation setting) | dB |
| 1 dB Compression[3,4] | | 1 MHz ≤ 1.2 GHz | 30 | 34 | - | dBm |
| Input IP3[1,2,4] | Two-tone inputs up to +18 dBm | 1 MHz ≤ 1.2 GHz | - | 52 | - | dBm |
| Return Loss | | 1 MHz ≤ 1.2 GHz | 10 | 13 | - | dB |
| Switching Time | 50% control to 0.5 dB of final value | | - | - | 1 | µs |

Notes: 1. Device Linearity will begin to degrade below 1Mhz
2. Max input rating in Table 1 & Figures on Pages 6 to 8 for data across frequency.
3. Note Absolute Maximum in Table 1.
4. Measured in a 50 Ω system.

## Switching Frequency

The PE43665 has a maximum 25 kHz switching rate.

Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states.

Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

# Programming Options

## Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE43665. The P/S bit provides this selection, with P/S=LOW selecting the parallel interface and P/S=HIGH selecting the serial interface.

## Parallel Mode Interface

The parallel interface consists of five CMOS-compatible control lines that select the desired attenuation state, as shown in Table 4.

The parallel interface timing requirements are defined by Figure 3 (Parallel Interface Timing Diagram), Table 8 (Parallel Interface AC Characteristics), and switching speed (Table 3).

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 3) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

## Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 2 (Serial Interface Timing Diagram) and Table 7 (AC Characteristics).

## Power-up Control Settings

The PE43665 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S=1), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S=0) with LE=0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in Table 5 (Power-Up Truth Table, Parallel Mode).

**Table 4 • *Truth Table***

| P/S | C16 | C8 | C4 | C2 | C1 | C0.5 | Attenuation State |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reference Loss |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.5 dB |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 dB |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2 dB |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4 dB |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8 dB |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 16 dB |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 31.5 dB |

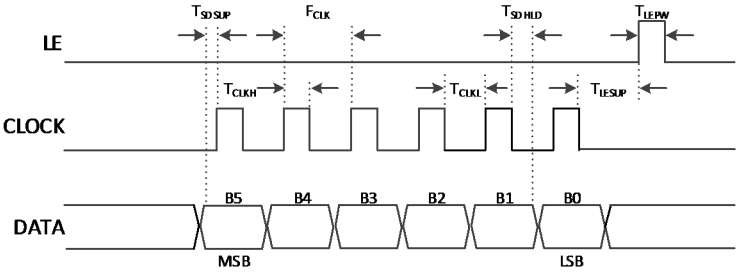
Note: Not all 64 possible combinations of C0.5-C16 are shown in table

**Table 5 • *Parallel PUP Truth Table***

| P/S | LE | PUP2 | PUP1 | Attenuation State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reference Loss |
| 0 | 0 | 1 | 0 | 8 dB |
| 0 | 0 | 0 | 1 | 16 dB |
| 0 | 0 | 1 | 1 | 31 dB |
| 0 | 1 | X | X | Defined by **C0.5-C16** |

Note: Power up with LE=1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active.

## Figure 2 • *Serial Interface Timing Diagram*

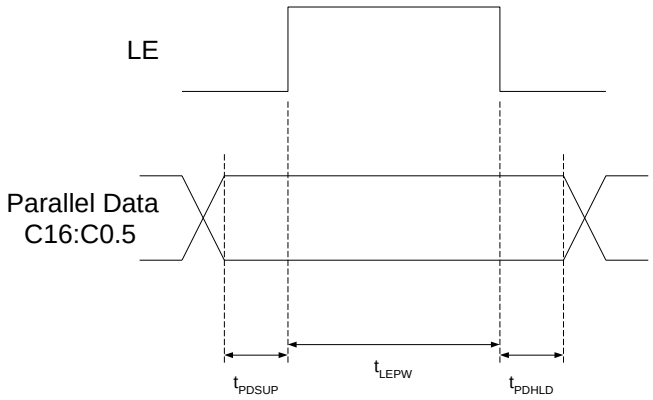



## Table 6 • *6-Bit Attenuator Serial Programming*

| B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|
| C16 | C8 | C4 | C2 | C1 | C0.5 |

MSB (first in) LSB (last in)

## Figure 3 • *Parallel Interface Timing Diagram*




## Table 7 • *Serial Interface AC Characteristics*

$V_{DD}$ = 3.0 V, -40° C < $T_A$ < 85° C, unless otherwise specified

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{Clk}$ | Serial data clock frequency (Note 1) | | 10 | MHz |
| $t_{ClkH}$ | Serial clock HIGH time | 30 | | ns |
| $t_{ClkL}$ | Serial clock LOW time | 30 | | ns |
| $t_{LESUP}$ | LE set-up time after last clock falling edge | 10 | | ns |
| $t_{LEPW}$ | LE minimum pulse width | 30 | | ns |
| $t_{SDSUP}$ | Serial data set-up time before clock rising edge | 10 | | ns |
| $t_{SDHLD}$ | Serial data hold time after clock falling edge | 10 | | ns |

Note: $f_{Clk}$ is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify $f_{clk}$ specification.

## Table 8 • *Parallel Interface AC Characteristics*

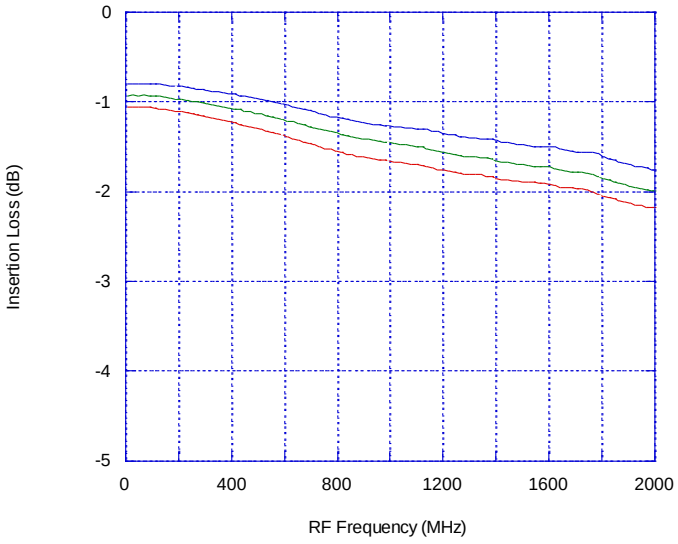
$V_{DD}$ = 3.0V, -40°C < $T_A$ < 85°C, unless otherwise specified

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{LEPW}$ | LE minimum pulse width | 10 | | ns |
| $t_{PDSUP}$ | Data set-up time before rising edge of LE | 10 | | ns |
| $t_{PDHLD}$ | Data hold time after falling edge of LE | 10 | | ns |

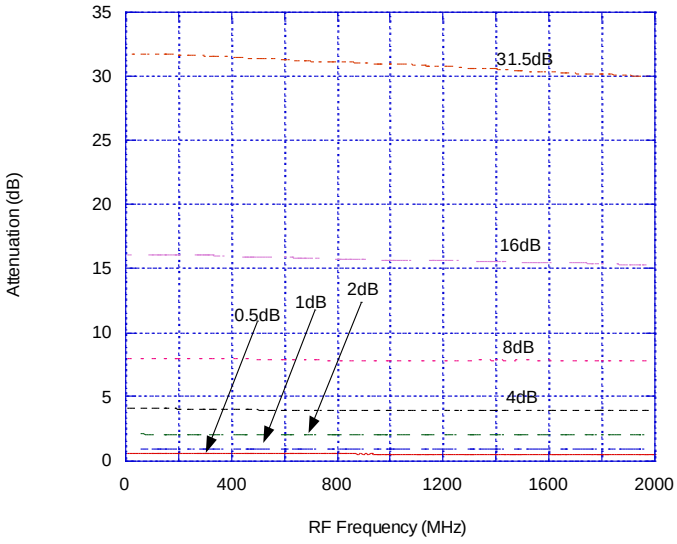
# Typical Performance Data

Figure 4–Figure 14 show the typical performance data at 25°C, $V_{DD}$ = 3.0V unless otherwise specified.

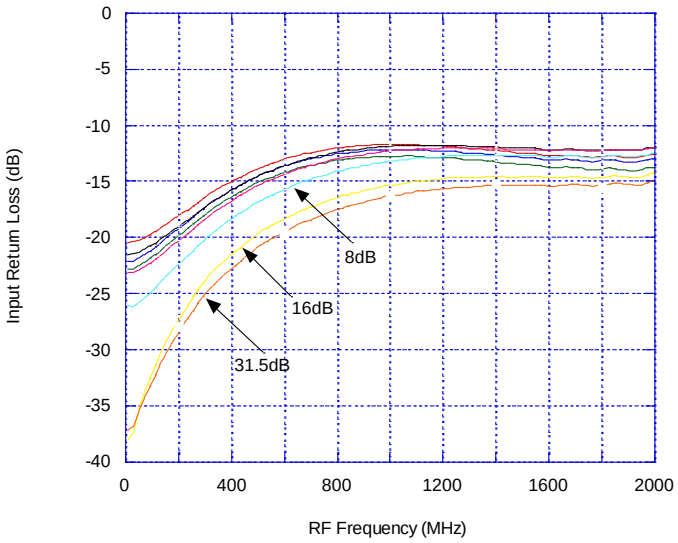
## Figure 4 • *Insertion Loss*



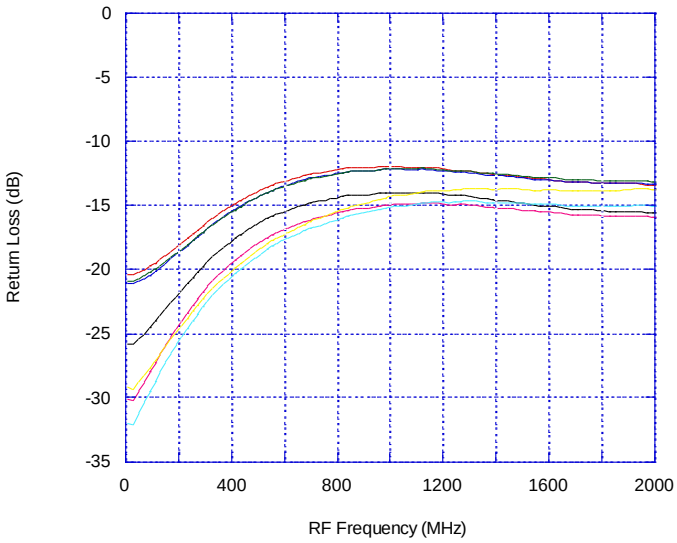

## Figure 5 • *Attenuation at Major steps*



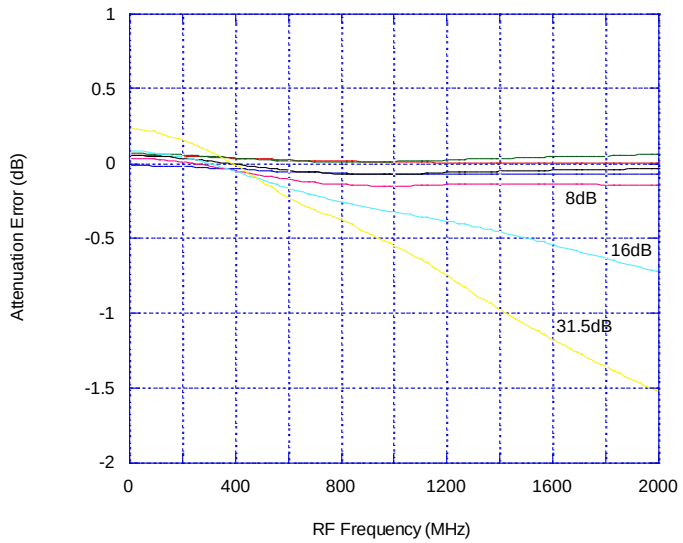

## Figure 6 • *Input Return Loss at Major Attenuation Steps*



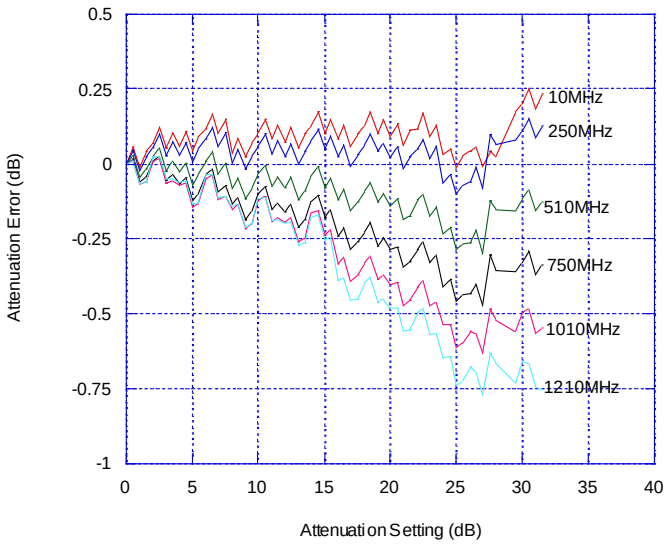

## Figure 7 • *Output Return Loss at Major Attenuation Steps*



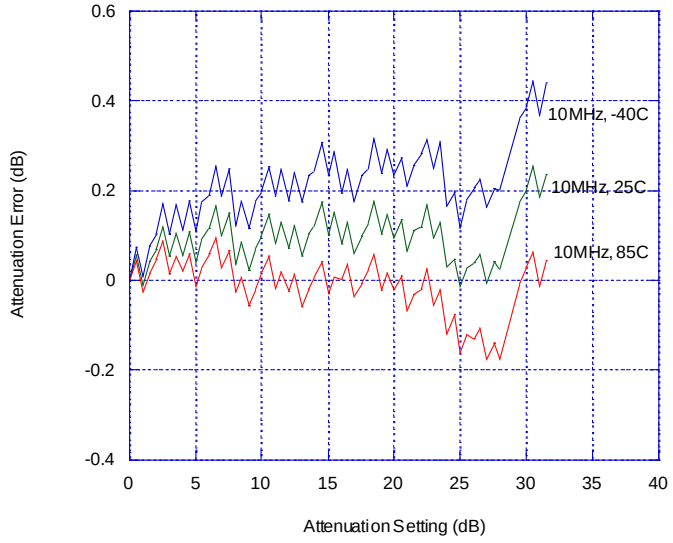
## Figure 8 • *Attenuation Error Vs. Frequency*



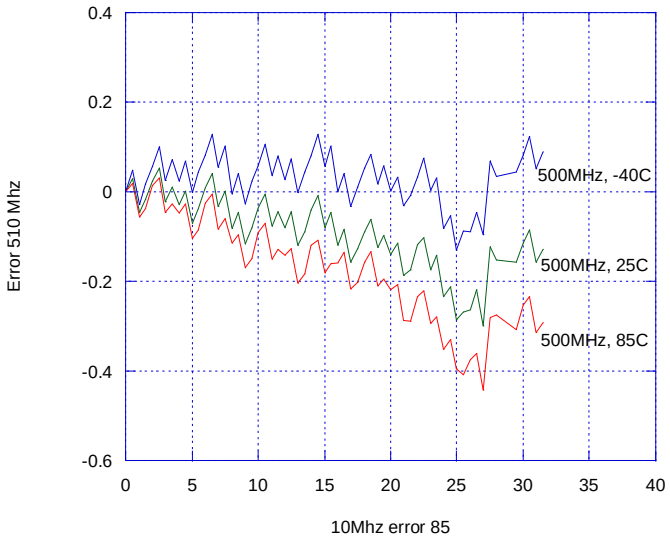

## Figure 9 • *Attenuation Error Vs. Attenuation Setting*




## Figure 10 • *Attenuation Error Vs. Attenuation Setting*



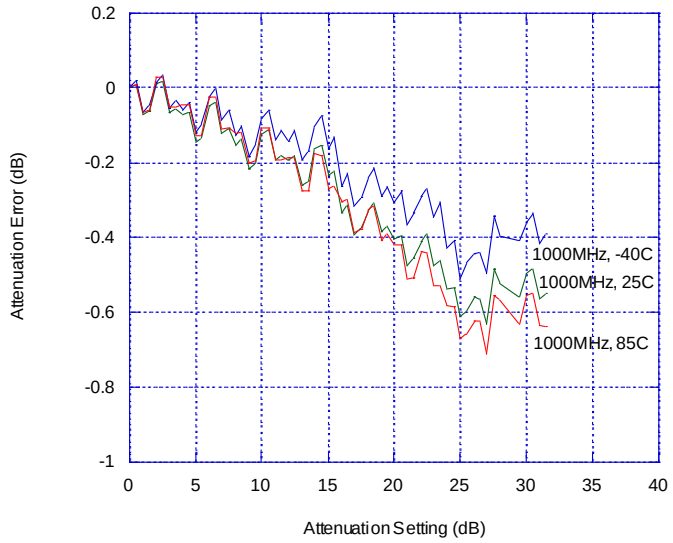

## Figure 11 • *Attenuation Error Vs. Attenuation*



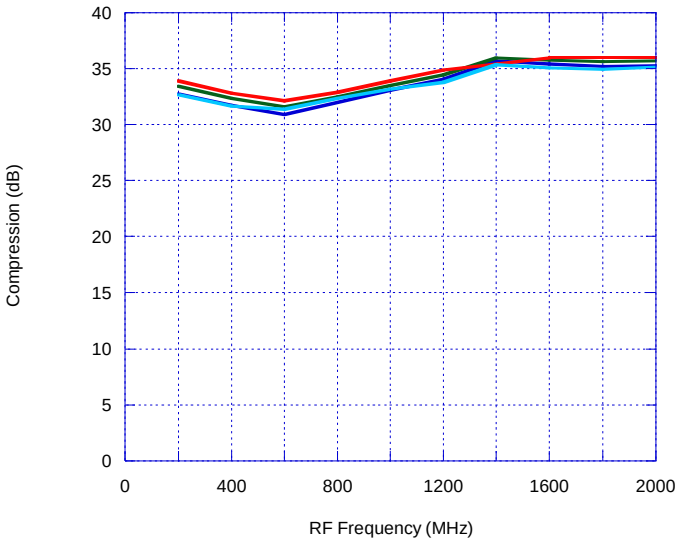

Note: Positive attenuation error indicates higher attenuation than target value

## *Typical Performance Data @ 25°C, $V_{DD}$ = 3.0 V*

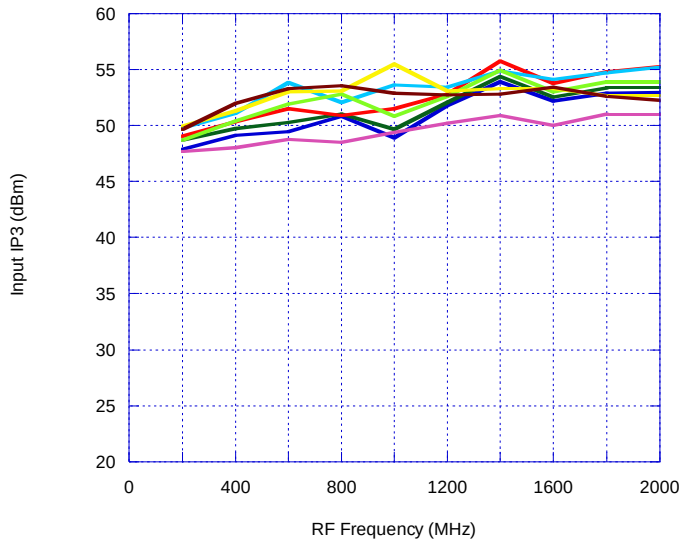
### Figure 12 • *Attenuation Error Vs. Frequency*




### Figure 13 • *Input 1 dB Compression*
(Major attenuation states, 50 Ω System)




### Figure 14 • *Input IP3 Vs. Frequency*
(Major attenuation states, 50 Ω System)

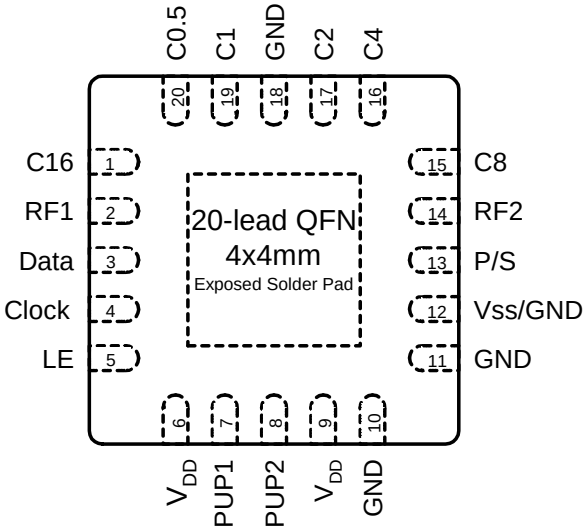



Note: Positive attenuation error indicates higher attenuation than target value

## Pin Information

This section provides pinout information for the PE43665. Figure 18 shows the pin map of this device for the available package. Table 9 provides a description for each pin.

### Figure 18 • *Pin Configuration (Top View)*




### Table 9 • *Pin Descriptions for PE43665*

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | C16 | Attenuation control bit, 16dB (Note 4). |
| 2 | RF1 | RF port (Note 1). |
| 3 | Data | Serial interface data input (Note 4). |
| 4 | Clock | Serial interface clock input. |
| 5 | LE | Latch Enable input (Note 2). |
| 6 | $V_{DD}$ | Power supply pin. |
| 7 | PUP1 | Power-up selection bit, MSB. |
| 8 | PUP2 | Power-up selection bit, LSB. |
| 9 | $V_{DD}$ | Power supply pin. |
| 10 | GND | Ground connection. |
| 11 | GND | Ground connection. |
| 12 | $V_{ss}$/GND | Negative supply voltage or GND connection (Note 3) |
| 13 | P/S | Parallel/Serial mode select. |
| 14 | RF2 | RF port (Note 1). |
| 15 | C8 | Attenuation control bit, 8 dB. |
| 16 | C4 | Attenuation control bit, 4 dB. |
| 17 | C2 | Attenuation control bit, 2 dB. |
| 18 | GND | Ground connection. |
| 19 | C1 | Attenuation control bit, 1 dB. |
| 20 | C0.5 | Attenuation control bit, 0.5 dB. |
| Paddle | GND | Ground for proper operation |

Note 1: Both RF ports must be held at 0 $V_{DC}$ or DC blocked with an external series capacitor.

2: Latch Enable (LE) has an internal 100 kΩ resistor to $V_{DD}$.

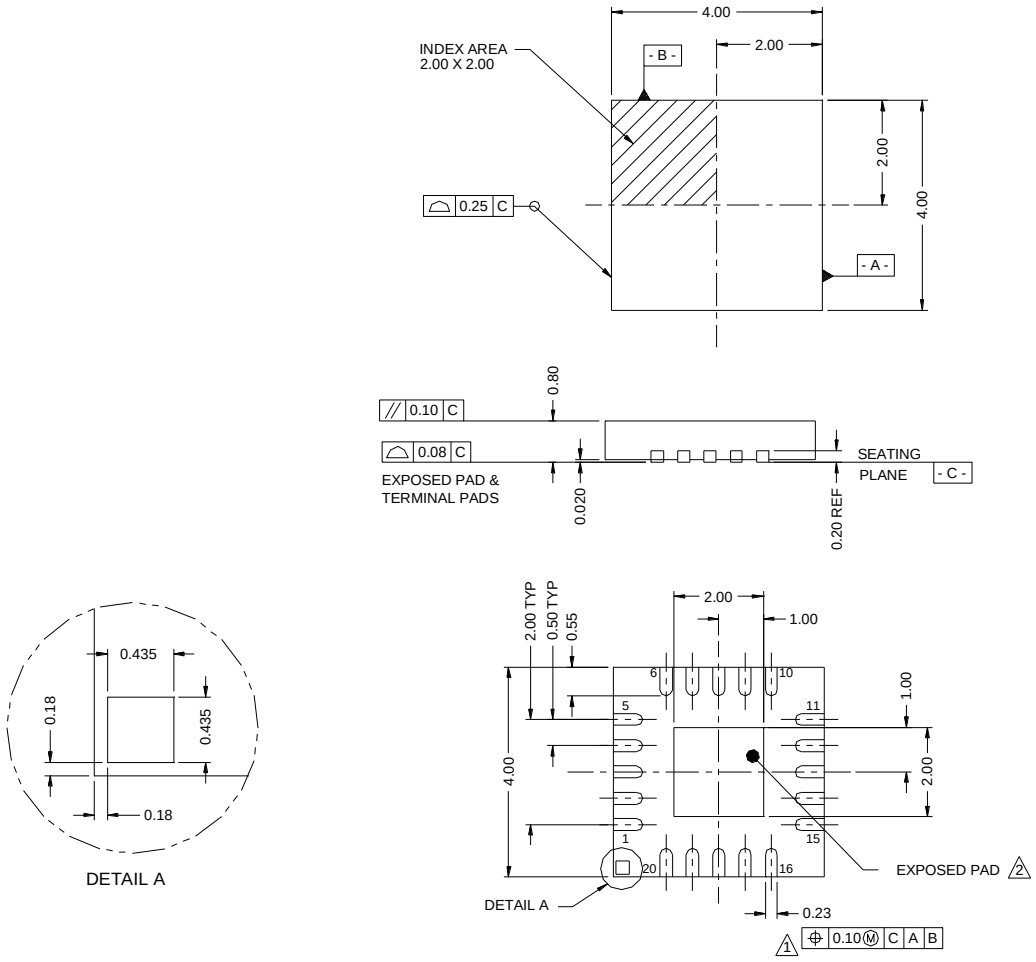
3: Connect pin 12 to GND to enable internal negative voltage generator. Connect pin 12 to $V_{SS}$ ($-V_{DD}$) to bypass and disable internal negative voltage generator.

4. Place a 10 kΩ resistor in series, as close to pin as possible to avoid frequency resonance.

### Resistor on Pin 1 & 3

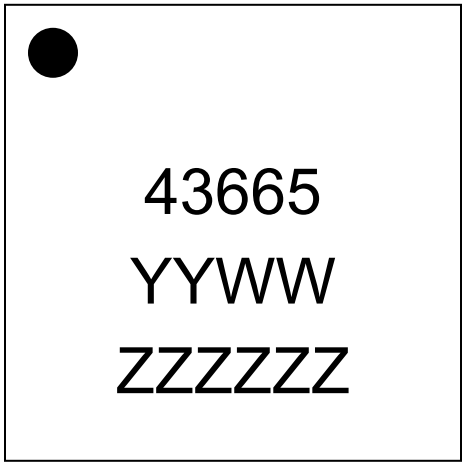
A 10 kΩ series resistor on the inputs to Pin 1 & 3 (see Figure 18) will eliminate package resonance between the RF input pin and the two digital inputs. Specified attenuation error versus frequency performance is dependent upon this condition.

## Figure 19 • *Package Drawing*




1. Dimension applies to metallized terminal and is measured between 0.25 and 0.30 from terminal tip.
2. Coplanarity applies to the exposed heat sink slug as well as the terminals.
3. Dimensions are in millimeters.

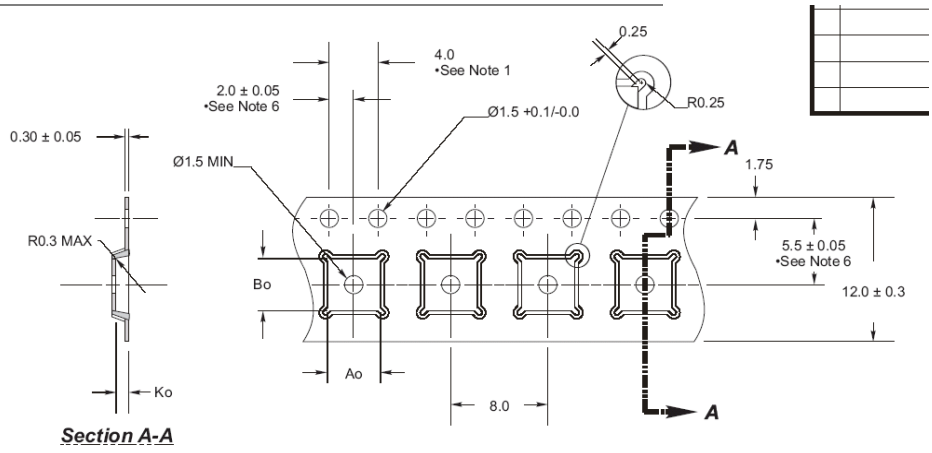
## Figure 20 • *Marking Specifications*




YYWW = Date Code

ZZZZZZ = Last six digits of lot number

## Figure 21 • *Tape and Reel Drawing*




Ao = 4.35 mm
Bo = 4.35 mm
Ko = 1.1 mm

Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

## Table 10 • *Ordering Information*

| Order Code | Description | Package | Shipping Method |
|---|---|---|---|
| PE43665A-Z | PE43665 Digital step attenuator | Green 20-lead 4x4mm QFN | 3000 units / T&R |
| EK43665-01 | PE43665 Evaluation kit | Evaluation Kit | 1 / Box |

## Document Categories

### Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### Preliminary Specification

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