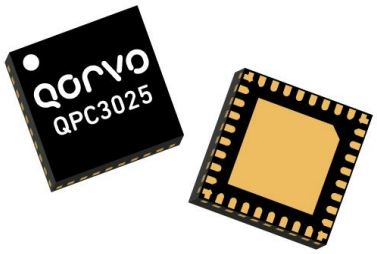
QPC3025

High Power, SOI, SPDT Switch

Product Overview

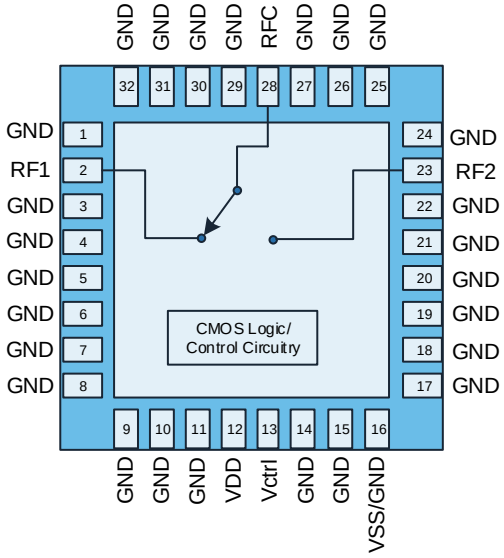
The QPC3025 is a Silicon on Insulator (SOI) single-pole, double-throw (SPDT) switch, designed for use in 4G/5G wireless infrastructure applications and other high performance communications systems. It offers low insertion loss in a symmetric topology with excellent linearity. The switch can handle up to 20W CW and 30W pulsed power with 50 Ohm load. No blocking capacitors are necessary on the RF ports. The switch ports are reflective. The QPC3025 is +1.8V logic compatible and has a single-pin solution to disable the Negative Voltage Generator and supply negative voltage from off-chip, if necessary.

The QPC3025 is packaged in a RoHS-compliant, compact 5x5 mm surface-mount leadless package.



32 Pin 5 mm x 5 mm leadless SMT Package

Functional Block Diagram



Top View

Key Features

- 30 MHz to 4200 MHz Operation
- Symmetric Switch Structure
- 0.35dB Insertion Loss at 2 GHz
- Power Handling: 30W pulsed power
  20W CW
- High Isolation: 39 dB at 2 GHz
- +1.8 V Logic Compatible
- HBM ESD Rating: Class 2 (2000V to <4000V)
- 2.7 – 5.5 V Supply Range

Applications

- Repeaters/Boosters
- Test and Measurement Equipment

Ordering Information

Part No.	Description
QPC3025TR13	2500 pcs on a 13” reel
QPC3025SR	100 pcs on a 7” reel
QPC3025EVB01	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-50 to 150 °C
V_{DD}	+6 V
V_{CTRL}	-0.3V to +6V
Pin, 80-2000 MHz	45.5 dBm
Pin, 2000-2700 MHz	45 dBm
Pin, 2700-4200 MHz	44 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD}	+2.7	+5	+5.5	V
V_{SS} (1)	-5.5	-5	-3.3	V
Pin (RFC – RFX), CW, 50 Ω			43	dBm
Pin (RFC – RFX) Pulsed with 10% DC, 5ms period, 50 Ω, 80-2000 MHz			45	dBm
Pin (RFC – RFX) Pulsed with 10% DC, 5ms period, 50 Ω, 2000-2700 MHz			44.5	dBm
Pin (RFC – RFX) Pulsed with 10% DC, 5ms period, 50 Ω, 2700-4200 MHz			43.5	dBm
T_{CASE}	−40		+85	°C
Tj at MTTF>10^6 hrs			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

1. For off-chip negative supply. Otherwise apply 0V to enable internal NVG.

Electrical Specifications

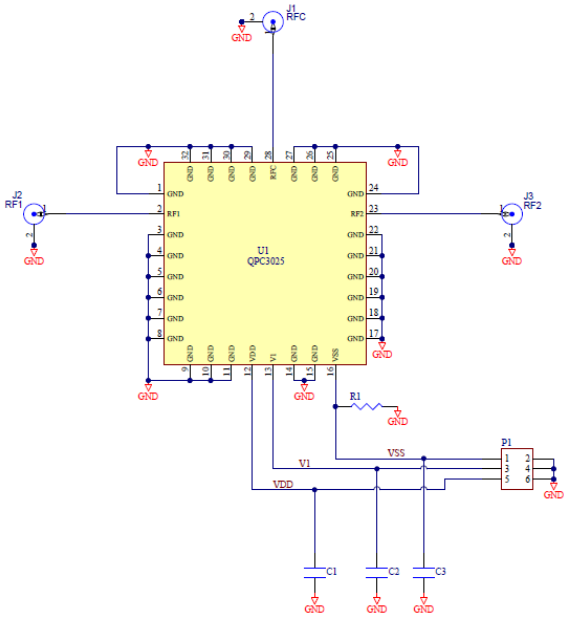
Test conditions, unless otherwise noted: Temp = 25°C, V_{DD} = +5V.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		30		4200	MHz
Insertion Loss (1)	30 - 1000 MHz		0.35		dB
	1000 – 2000 MHz		0.35		dB
	2000 - 3000 MHz		0.39		dB
	3000 – 4200 MHz		0.41		dB
Isolation, RFC-RFX (1)	30 - 1000 MHz		46		dB
	1000 – 2000 MHz		38.5		dB
	2000 - 3000 MHz		35		dB
	3000 – 4200 MHz		29		dB
Isolation, RFX-RFX (1)	30 - 1000 MHz		47.5		dB
	1000 – 2000 MHz		40		dB
	2000 - 3000 MHz		36		dB
	3000 – 4200 MHz		30		dB
Return Loss, RFC	30 - 1000 MHz		33		dB
	1000 – 2000 MHz		25		dB
	2000 - 3000 MHz		23		
	3000 – 4200 MHz		22		dB
Return Loss, RFX	30 - 1000 MHz		35		dB
	1000 – 2000 MHz		25		dB
	2000 - 3000 MHz		23		
	3000 – 4200 MHz		25		dB
Input P0.1dB (2)	80 – 2000 MHz		+45.5		dBm
	2000 – 2700 MHz		+45		dBm
	2700 – 4200 MHz		+44		dBm
Input IP3	RFC-RFX, 2000 MHz, 32dBm/tone, 1MHz Δf		74		dBm
Harmonics	$2F_0$, F_0 = 1GHz at +45dBm Pulsed power (10%DC, 5ms period)		-90		dBc
	$3F_0$, F_0 = 1GHz at +45dBm Pulsed power (10%DC, 5ms period)		-87		dBc
Switching Time	Turn-on, (50% V_{CTRL} to 90% RF)		5.8		µs
	Turn-off, (50% V_{CTRL} to 10% RF)		4.7		µs
Settling Time	50% V_{CTRL} until harmonics settle to steady-state value		8.58		µs
Pin (hot switching)				15	dBm
Dead Time	Minimum time required between 50% V_{CTRL} (no RFin) to applying RFin > Pin (hot switching) level. (over operating temp range)		7		µs
Supply Current, I_{DD}	V_{DD} = +5V		90	200	µA
Control Voltage, V_{CTRL}	VIH	1.17		V_{DD}	V
	VIL	0		0.63	V
Control Current, I_{CTRL}			2		µA
Negative Supply Current, I_{SS}	Pin 16, V_{SS} = -5V		-100		µA
Spur Level (3)	Any RF ports, V_{SS} = 0V, NVG ON		-115		dBm
Thermal Resistance			17		°C/W

Notes:

1. Production test screen is done at 1000MHz and 2000MHz only.
2. This is just a linearity figure of merit. Refer to 'Recommended Operating Conditions' table for Pin levels.
3. If spur-free performance is desired the internal NVG can be disabled by supplying an external negative voltage at pin 16.

Application Circuit Schematic and Layout



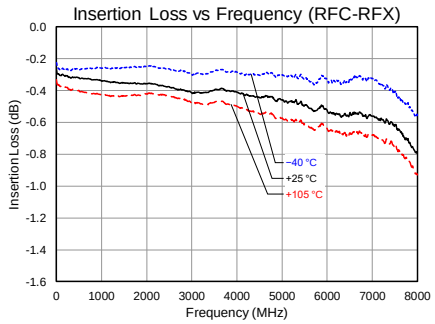
Bill of Material

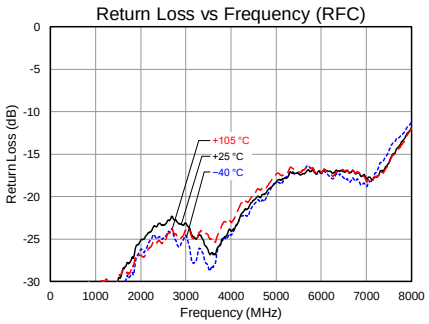
Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	High Power SPDT Switch	Qorvo	QPC3025
C1	0.1 uF	CAP, 0402, 50V, 10%, X7R	Various	
C2	100 pF	CAP, 0402, 50V, 10%	Various	
R1	1 MΩ	RES, 0402, 5%, 1/16W	Various	

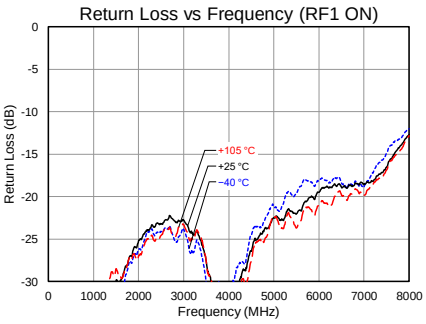
Logic Table

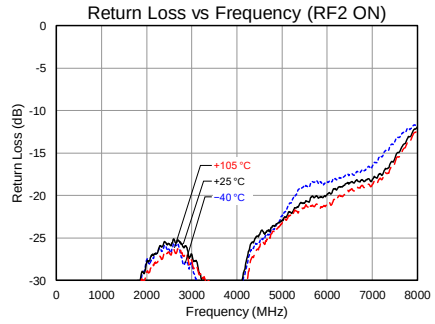
Vctrl	Switch path
0	RFC-RF2
1	RFC-RF1

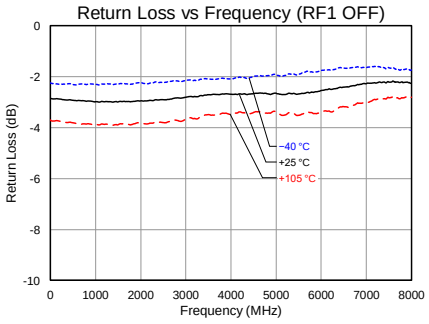
Performance Plots

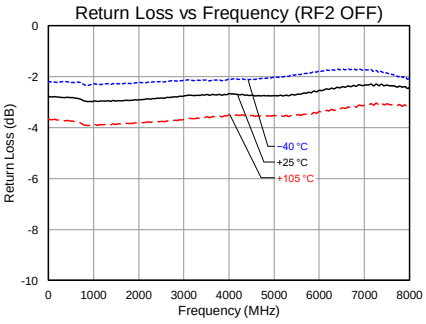


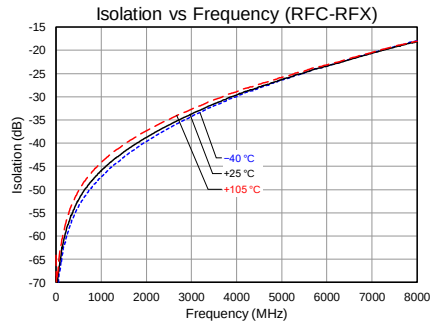


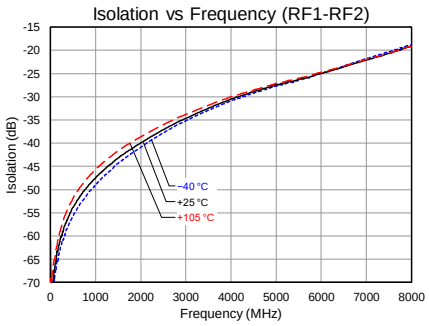




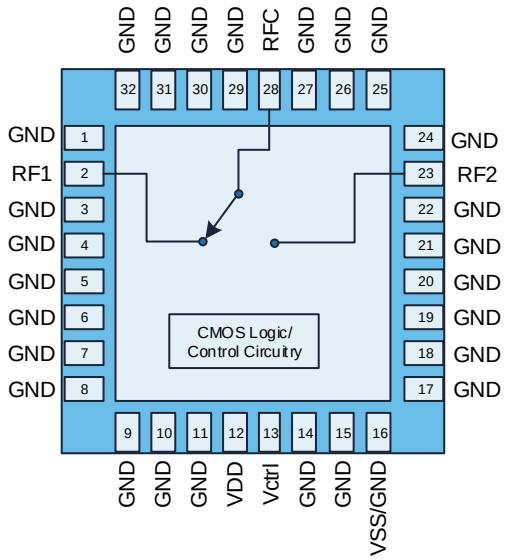








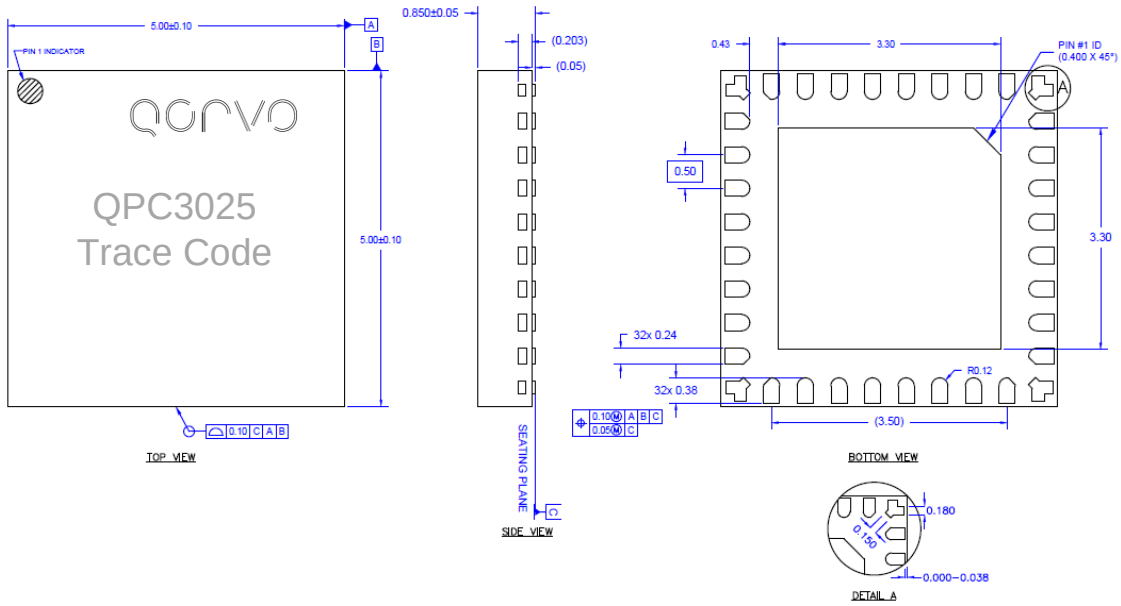
Pin Configuration and Description



Top View

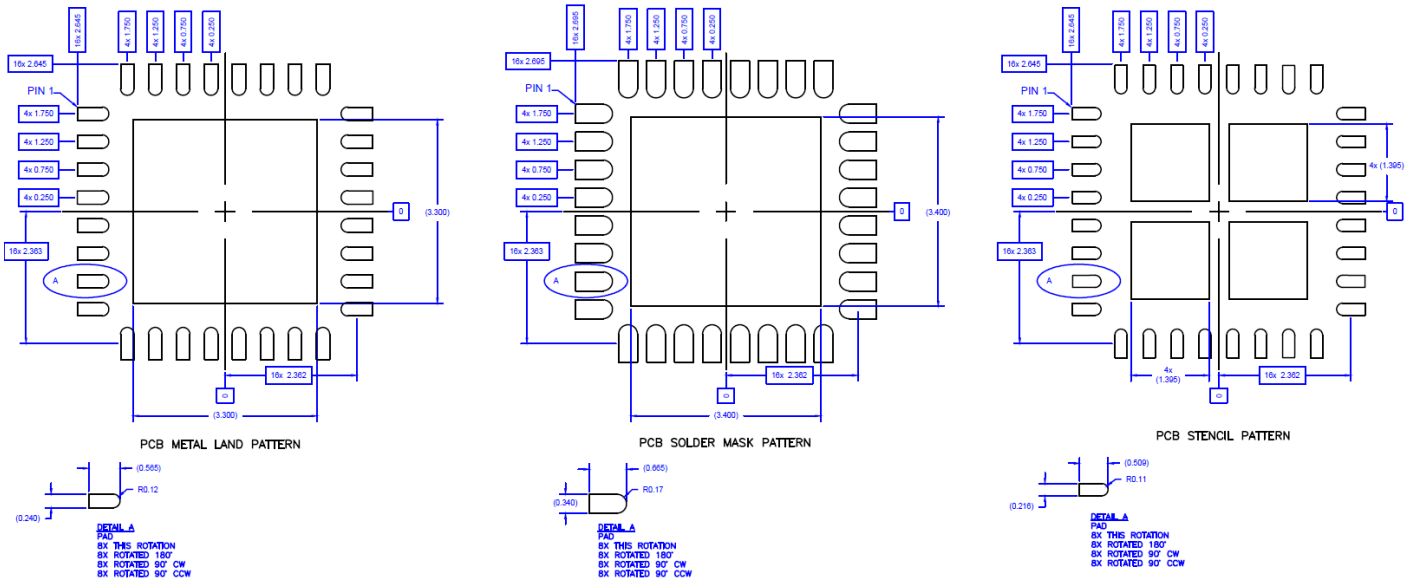
Pin No.	Label	Description
1,3,4,5,6,7,8,9,10,11,14, 15,17,18,19,20,21,22,24, 25,26,29,31,32	GND	No internal connection but recommend to ground on board for proper mounting integrity.
27,30	GND	Internally connected and must be grounded on board.
2	RF1	Switch output port 1. Internally at 0V DC.
28	RFC	Switch common port. Internally at 0V DC.
23	RF2	Switch output port 2. Internally at 0V DC.
13	V_{CTRL}	Switch control voltage
12	VDD	Supply voltage. Bypassing recommended.
16	VSS/GND	Negative Voltage Generator (NVG) control pin. Supply GND (Low inductive path to ground) to enable internal NVG or supply −3.3 V to −5.5 V to disable internal NVG. Once disabled, internal NVG cannot be enabled without cycling VDD.
Backside Pad	GND	Ground connection. The back side of the package should be soldered to a good ground pad with enough vias for thermal dissipation and RF/DC ground path.

Package Marking and Dimensions



Notes:
1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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